Monday 17th March

08.30 Registration

09.00 Workshop Opening

09.15 **Steve Trimberger, Xilinx, USA**[1]
Defect Avoidance in Programmable Devices

10.05 Yang Lin, Mark Zwolinski and Basel Halak, University of Southampton, UK
An Energy-Efficient Radiation Hardened Register File Architecture for Reliable Microprocessors

10.30 Tea/Coffee

10.50 **Martin Trefzer, University of York, UK**
Sense, Adapt, Survive: An Evolutionary Hardware Perspective

11.40 Andrey Mokhov, Newcastle University, UK
Algebraic Modelling of Switching Networks with Uncertainty

12.05 B. Chagun Basha and Sebastien Pillement, University of Rennes 1 & University of Nantes, France
New Reliable Reconfigurable FPGA Architecture for Safety and Mission Critical Applications

12.30 Lunch

14.00 **Sani Nassif, Radyalis, USA**
Medical Treatment For Variability: Lessons from Circuits Applied to Cancer Radiation Therapy

14.50 Hossein Mamaghanian, Giovanni Ansaloni, Mohamed M. Sabry, David Atienza and Pierre Vandergheynst, Ecole Polytechnique Federale de Lausanne, Switzerland
Hardware-Software Inexactness in Noise-aware Design of Low-Power Body Sensor Nodes

15.15 Andrew C. R. Angus, Fikru Adamu-Lema, Asen Asenov, Binjie Cheng, Campbell Millar, Neil Munro, Alan Murray, John Pennock and Neil Rankin, University of Edinburgh, University of Glasgow, Wolfson Microelectronics & Gold Standard Simulations, UK
Variation is the Future

15.40 Tea/Coffee

16.00 Aadithya V. Karthik, Sriramkumar Venugopalan, Alper Demir and Jaijeet Roychowdhury, University of California, Berkeley, USA & Koc University, Turkey
MUSTARD: A Technique for Designing SRAMs and DRAMs in the presence of Random Telegraph Noise

16.25 Mahdi Jelodari Mamaghani and Jim D. Garside, The University of Manchester, UK
High-Level Synthesis of GALS Systems

19.00 Social Event: York Terror Trail (meet outside The Golden Fleece Inn, see location map)

[1] Invited speakers are indicated by bold text

Tuesday 18th March

09.00 Registration

09.15 **Peter Cheung, Imperial College London, UK**
On-silicon Instrumentation - An Approach to Alleviate the Variability Problem

10.05 Edward Stott, Joshua M. Levine, George Constantinides and Peter Y. K. Cheung, Imperial College London, UK
Timing and Fault Instrumentation with Shadow Registers

10.30 Tea/Coffee

10.50 **Robert Aitken, ARM, USA**
Predictive Technology for Advanced Node Design Exploration

11.40 Negar Miralaei, Jyothish Soman and Timothy Jones, University of Cambridge, UK
PAM: A Processor Ageing Model Based on Critical Path Delays

12.05 Jie Ding, Dave Reid, Plamen Asenov, Campbell Millar and Asen Asenov, University of Glasgow, Gold Standard Simulations & ARM UK
Evaluating the impact of ageing on SRAM stability using accurate statistical Compact Models

12.30 Lunch

14.00 **Asen Asenov, University of Glasgow, UK**
Device-Technology Co-Optimisation (DTCO) in the Presence of Acute Variability

14.50 Hassan Ghasemzadeh Mohammadi, Pierre-Emmanuel Gaillardon and Giovanni De Micheli, Ecole Polytechnique Federale de Lausanne, Switzerland
Fast Process Variation Analysis in Emerging Nano-Scaled Technologies

15.15 Shida Zhong, Saqib Khursheed and Bashir M. Al-Hashimi, University of Southampton & University of Liverpool, UK
Variation-aware Fault Modelling and Simulation for Deep-Submicron Manufacturing Defects

15.40 Tea/Coffee

16.00 Poster Session (next page for complete list)

19.00 Social Event: Meal at the National Railway Museum (see location map)

Tuesday 18th March, Poster Session 16:00 – 17:00

Bo Liu, Glyndwr University, UK
Handling Expensiveness in Electronic Design Optimisation: An Emerging Trend

Ashur Rafiev, A. Iliasov, A. Romanovsky, A. Mokhov, F. Xia and A. Yakovlev, Newcastle University, UK
Resource-driven Modelling of Complex Digital Systems with Uncertainty

Sara Zermani, Catherine Dezan, Reinhardt Euler and Jean-Philippe Diguet, Université de Bretagne Occidentale, France
Online Inference for Adaptive Diagnosis via Arithmetic Circuit Compilation of Bayesian Networks

Jaroslav Borecky, Pavel Vıt and Hana Kubatova, Czech Technical University in Prague, Czech Republic
Fault Recovery Method of Modular Systems based on Reconfigurations

Chris Winstead, Gopalakrishnan Sundararajany and Emmanuel Boutillon, Utah State University, USA & Universite de Bretagne Sud, France
A Case Study in Noise Enhanced Computing: Noisy Gradient Descent Bit Flip Decoding

Antonio Arnone and Christopher Crispin-Bailey, University of York, UK
Dark Silicon, comparing Wave Cores with Composite State Machines

Ian Gray, Neil Audsley and Andrea Acquaviva, University of York, UK & Politecnico di Torino, Italy
Designing variability-aware embedded systems: The ToucHMore approach

G. Kalogeridou, N. Sklavos and A. W. Moore, Technological Educational Institute of Western Greece
A Hardware Trojan Detection Framework

Hossein Mamaghanian, Giovanni Ansaloni, Mohamed M. Sabry, David Atienza and Pierre Vandergheynst, Ecole Polytechnique Federale de Lausanne, Switzerland
Hardware-Software Inexactness in Noise-aware Design of Low-Power Body Sensor Nodes

Satish Grandhi, Satish Grandhi, Jiaoyan Chen, Christian Spagnol, David Mccarthy and Emanuel Popovici, University College Cork, Ireland
Innovative Reliable Chip Designs from Low-Powered Unreliable Components

Pedro Campos, David Lawson, Yuan Wang, Yang Xiao, Martin A. Trefzer, Simon J. Bale, James A. Walker and Andy M. Tyrrell, University of York, UK
Programmable Analogue and Digital Array (PAnDA)

Basel Halak, Teng Ma and Wei Ximeng, University of Southampton, UK
High Throughput CDMA communication architecture for many cores systems

Aadithya V. Karthik, Sriramkumar Venugopalan, Alper Demir and Jaijeet Roychowdhury, University of California, Berkeley, USA & Koc University, Turkey
MUSTARD: A Technique for Designing SRAMs and DRAMs in the presence of Random Telegraph Noise

B. Chagun Basha and Sebastien Pillement, University of Rennes 1 & University of Nantes, France
New Reliable Fault Tolerant FPGA Architecture: A Design for Mission Critical Applications

Wednesday 19th March

09.00 Registration

09.15 **Bashir Al-Hashimi, University of Southampton, UK**
Hardware Reliability of Embedded Systems

10.05 Martin A. Trefzer, Simon J. Bale, James A. Walker and Andy M. Tyrrell, University of York, UK
Fighting Stochastic Variability in a D-type Flip-Flop with Transistor-Level Reconfiguration

10.30 Tea/Coffee

10.50 **Roger Woods, Queen's University Belfast, UK**
FPGA-based realizations of embedded systems

11.40 Andrew D. Brown, R. Mills, K.J. Dugan, J.S. Reeve and S.B. Furber, University of Southampton & The University of Manchester, UK
Reliable computation with unreliable computers

12.05 Husni Habal and Helmut Graeb, Technische Universitat Munchen, Germany
Automatic MOSFET Sizing to Maximize the Lifetime Yield of Analog Circuits

12.30 Lunch

14.00 **Steve Johnson, University of York, UK**
Hybrid Biomolecular Electronic Devices

14.50 Fernando Rodríguez Salazar and Scott Roy, University of Glasgow, UK
Passive Skew Amplification in On-Chip Communication Links

15.15 Bert Moons and Marian Verhelst, KU Leuven, Belgium
The Influence of Spatial and Transient Circuit Variations on Energy and Accuracy in Stochastic Computing Circuits

15.40 Closing Remarks, followed by Tea/Coffee