

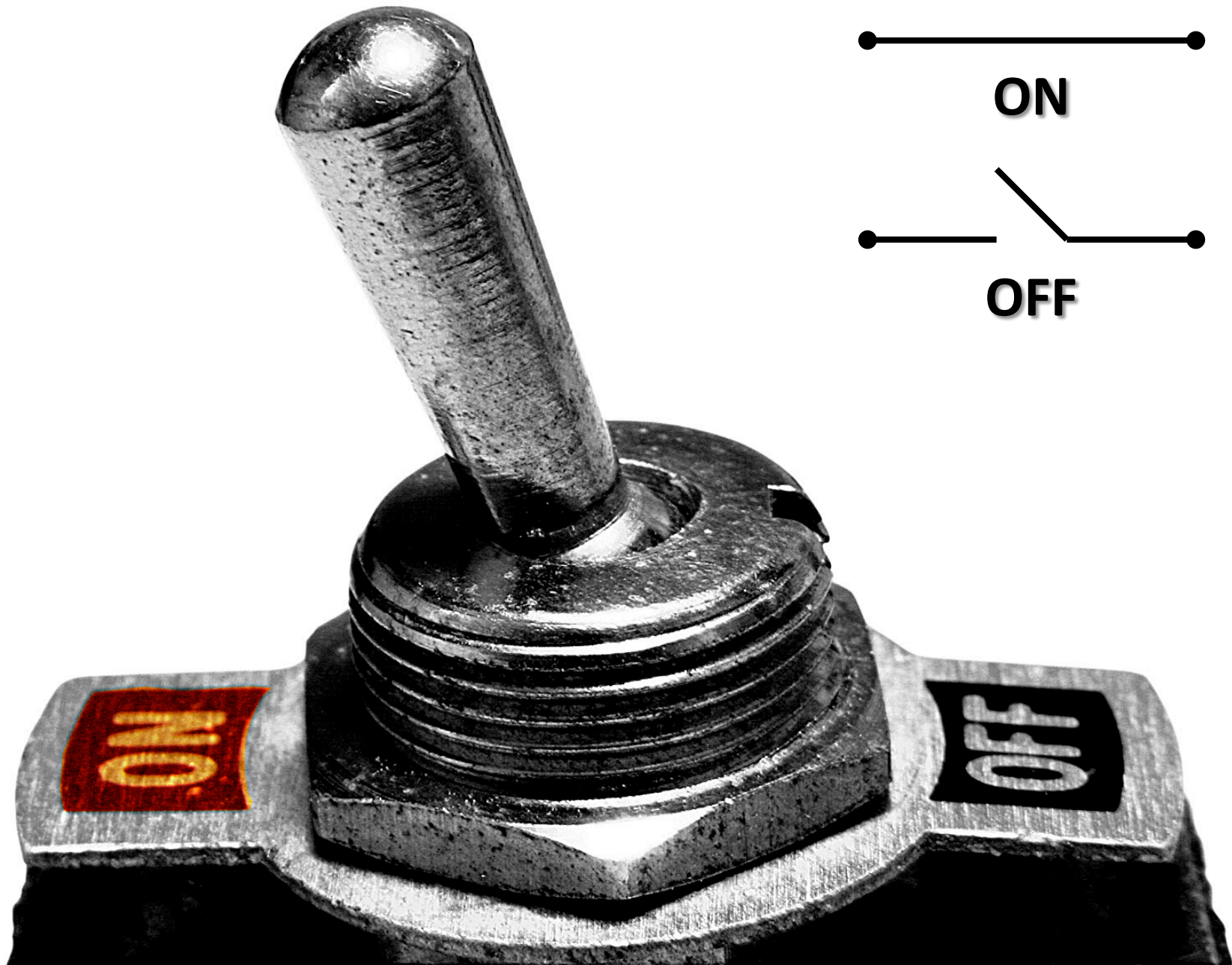
Algebraic Modelling of Switching Networks with Uncertainty

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Newcastle University, UK

Part I: The Switch

“The first light switch employing *quick-break technology* was invented by *John Henry Holmes* in 1884 in the Shieldfield district of Newcastle upon Tyne.”

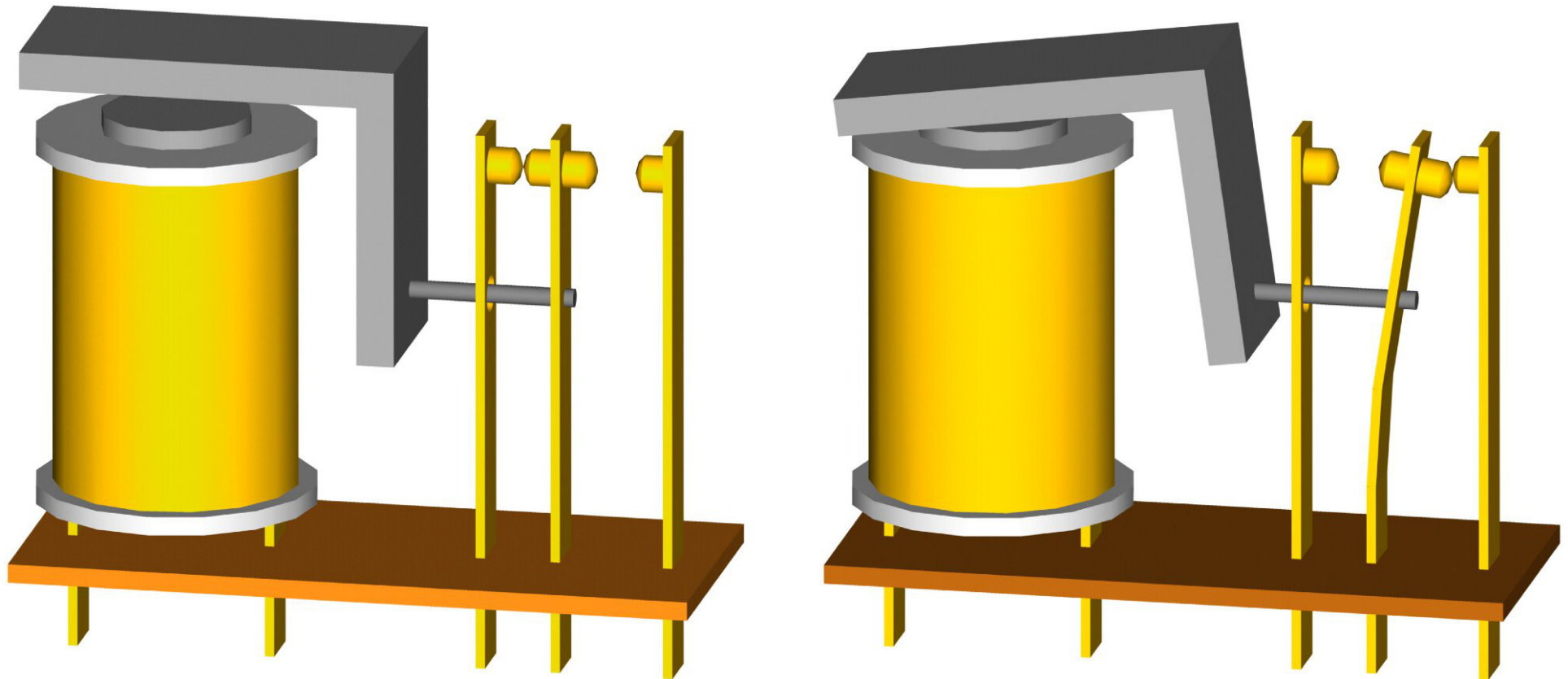
Wikipedia



ON

OFF

Relay: electrically operated switch



Smaller, faster, cheaper

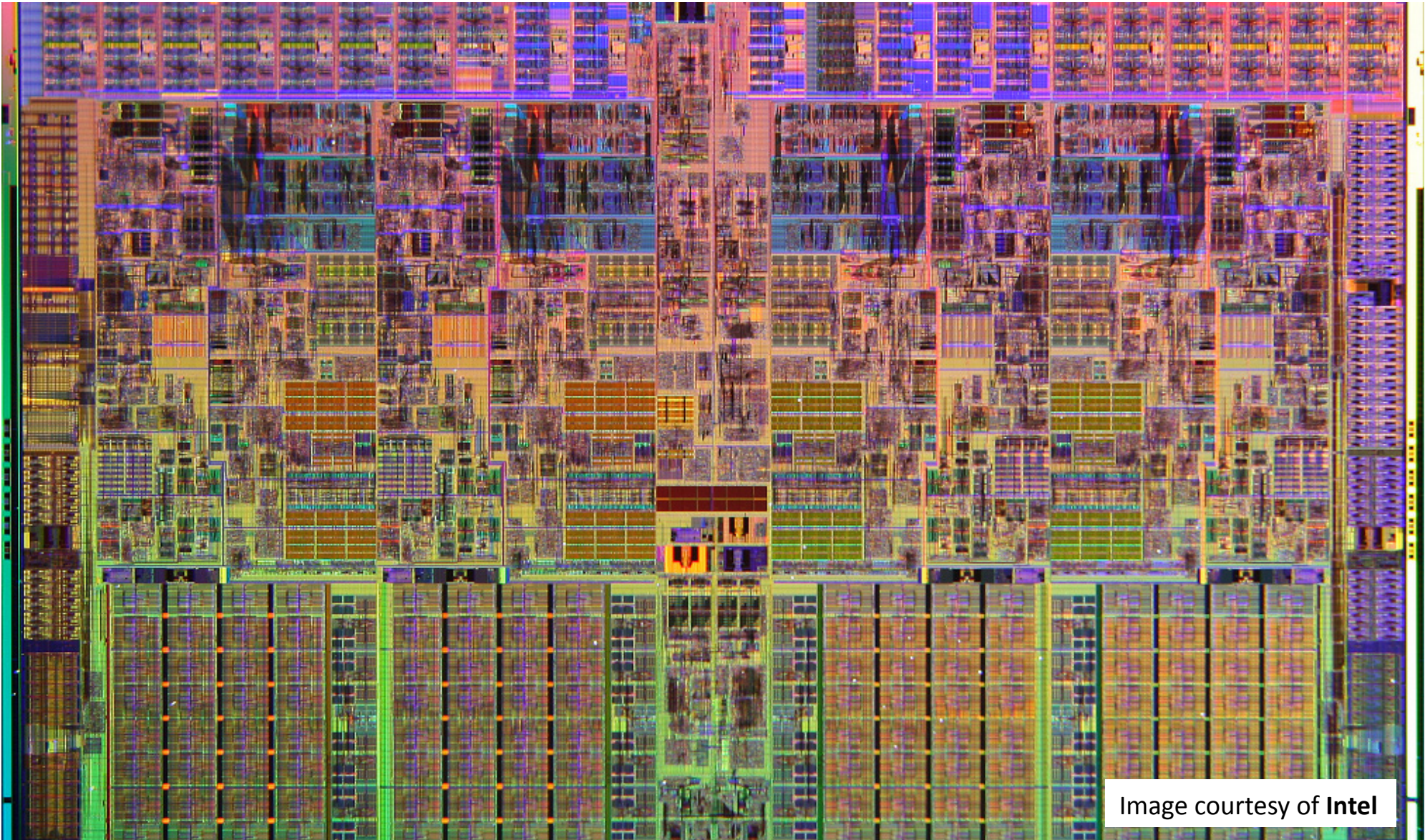


Image courtesy of Intel

Smaller, faster, cheaper

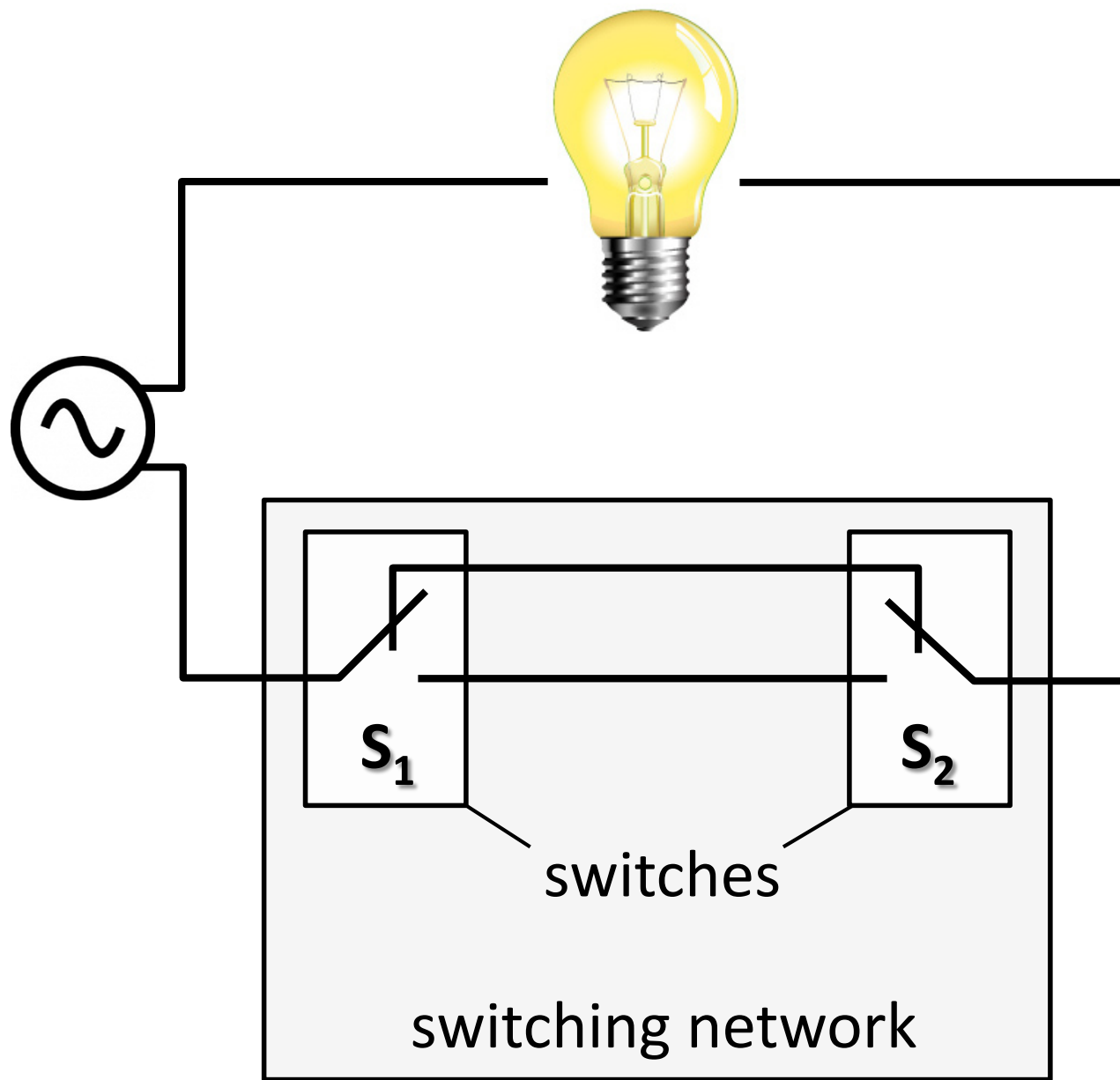
2 300 000 000
transistors

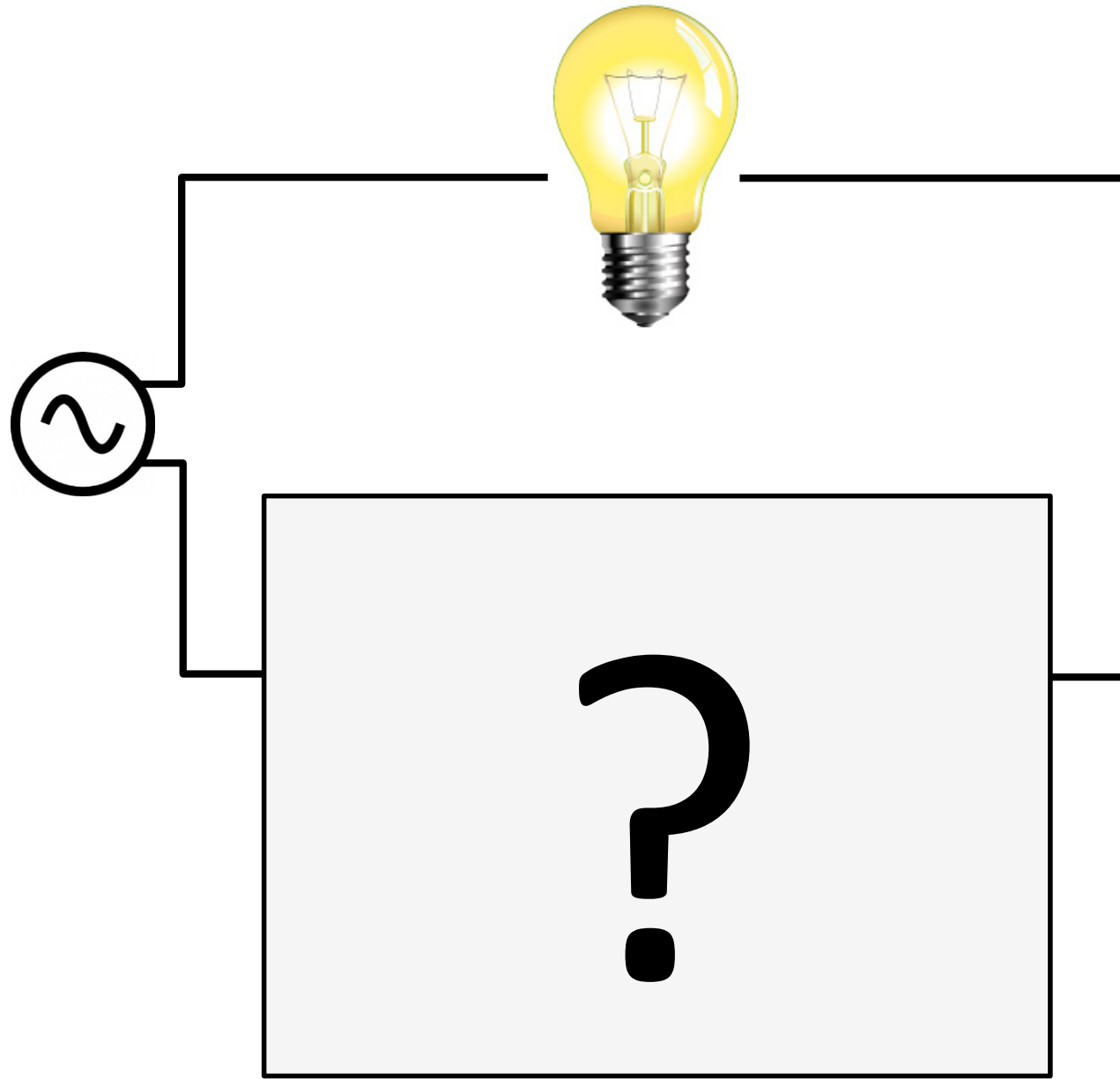
2 400 000 000
Hz

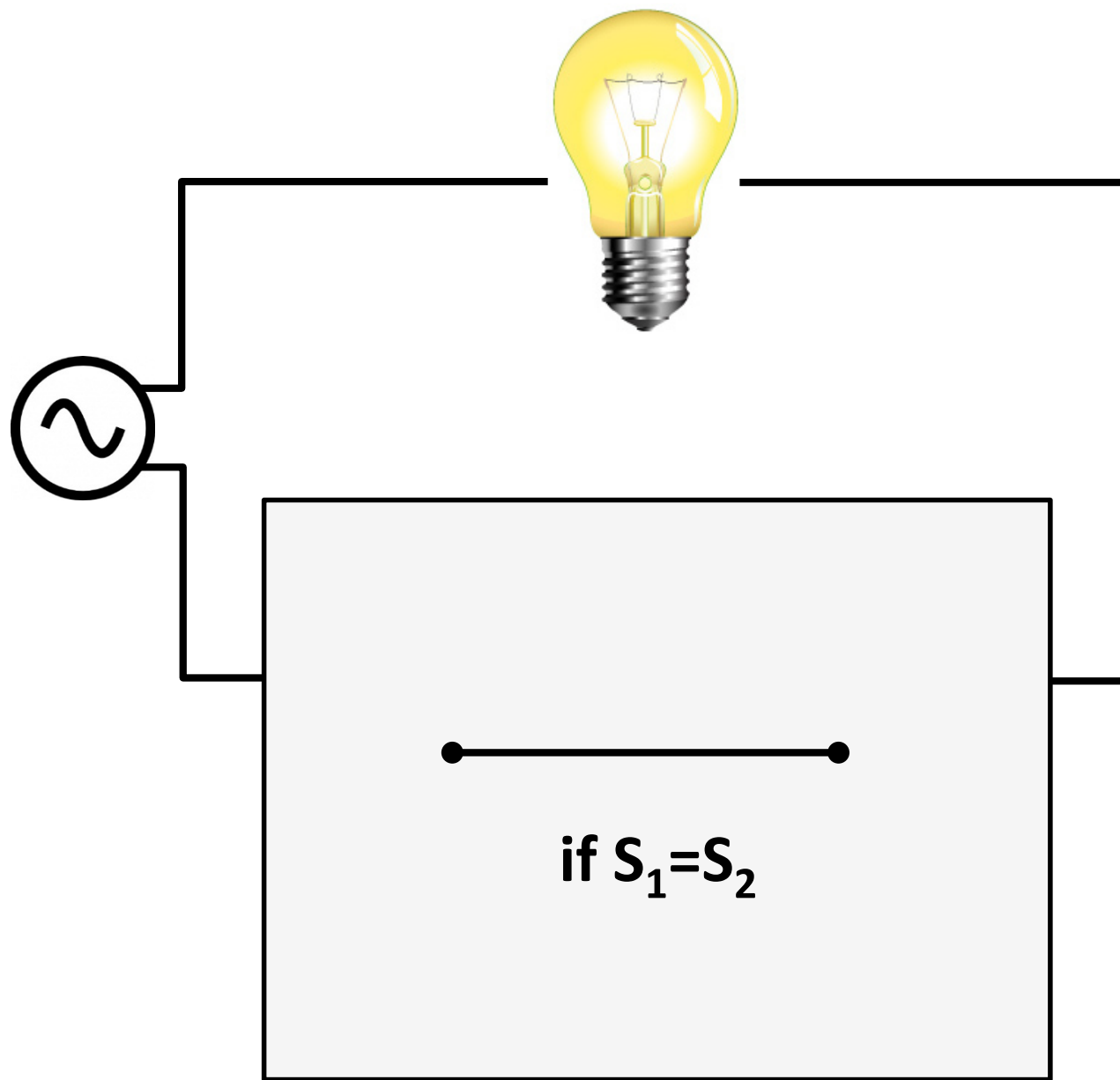
2 000 000 000
computers

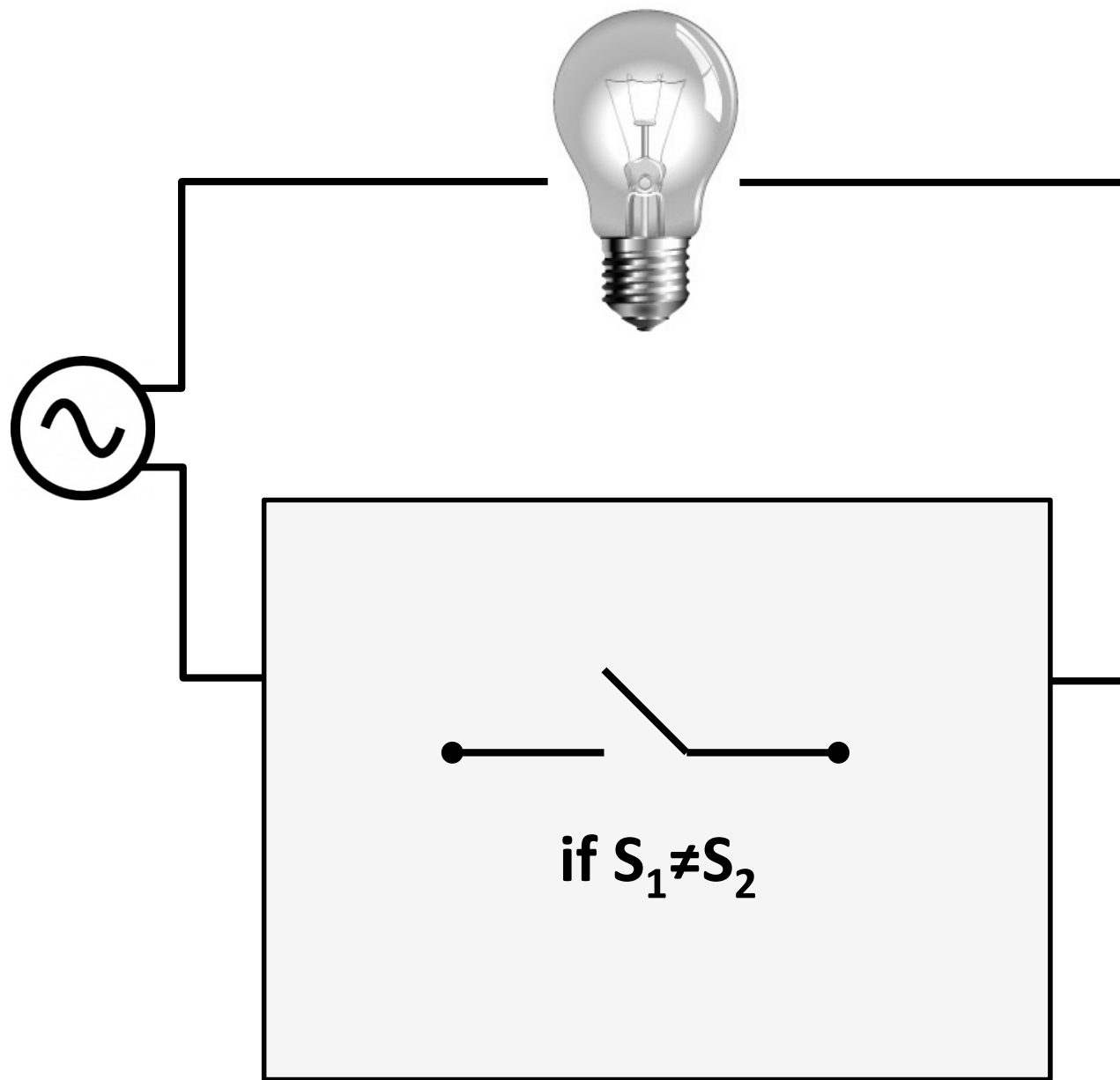
Image courtesy of Intel

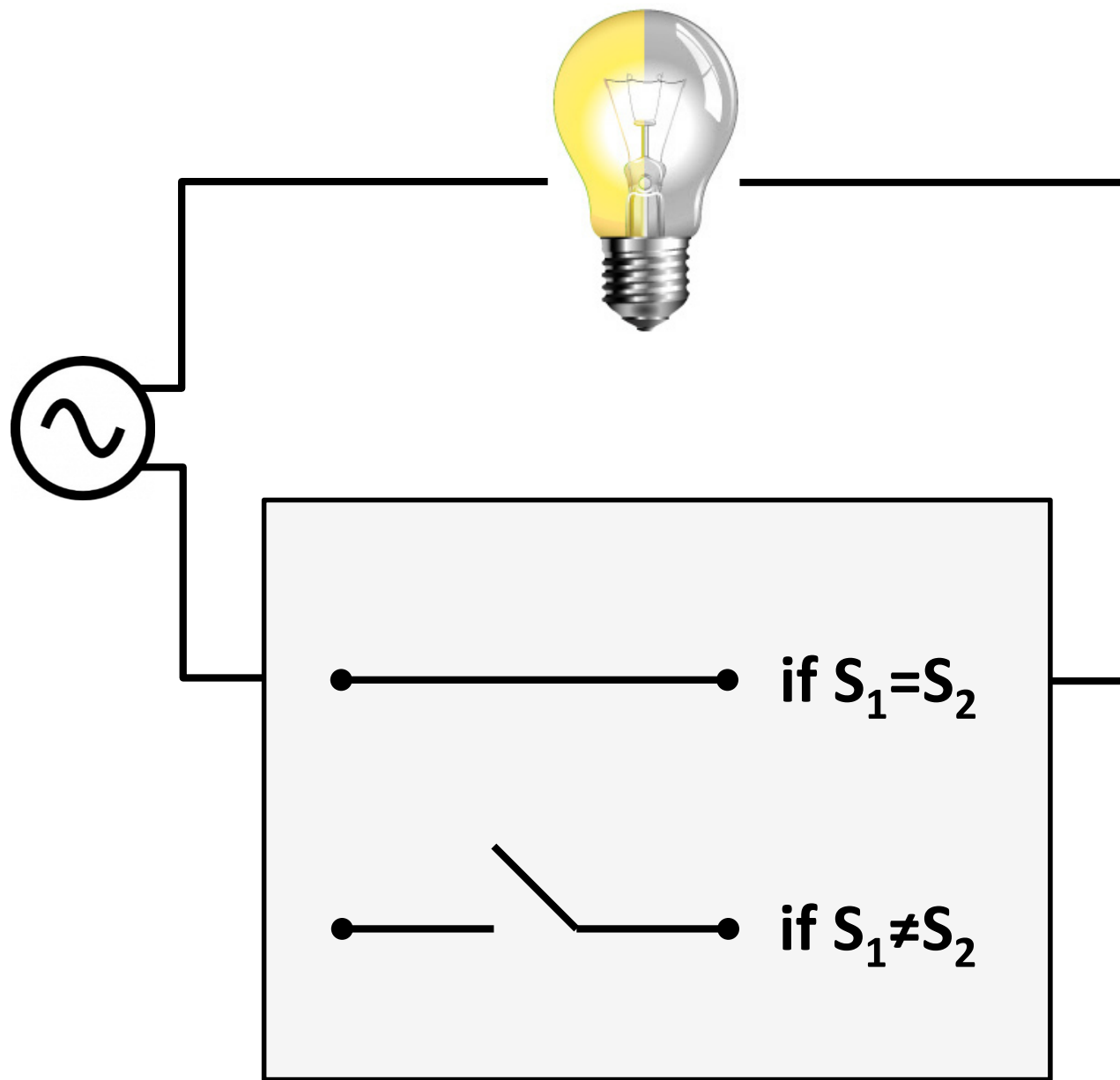
Part II: Switching Networks

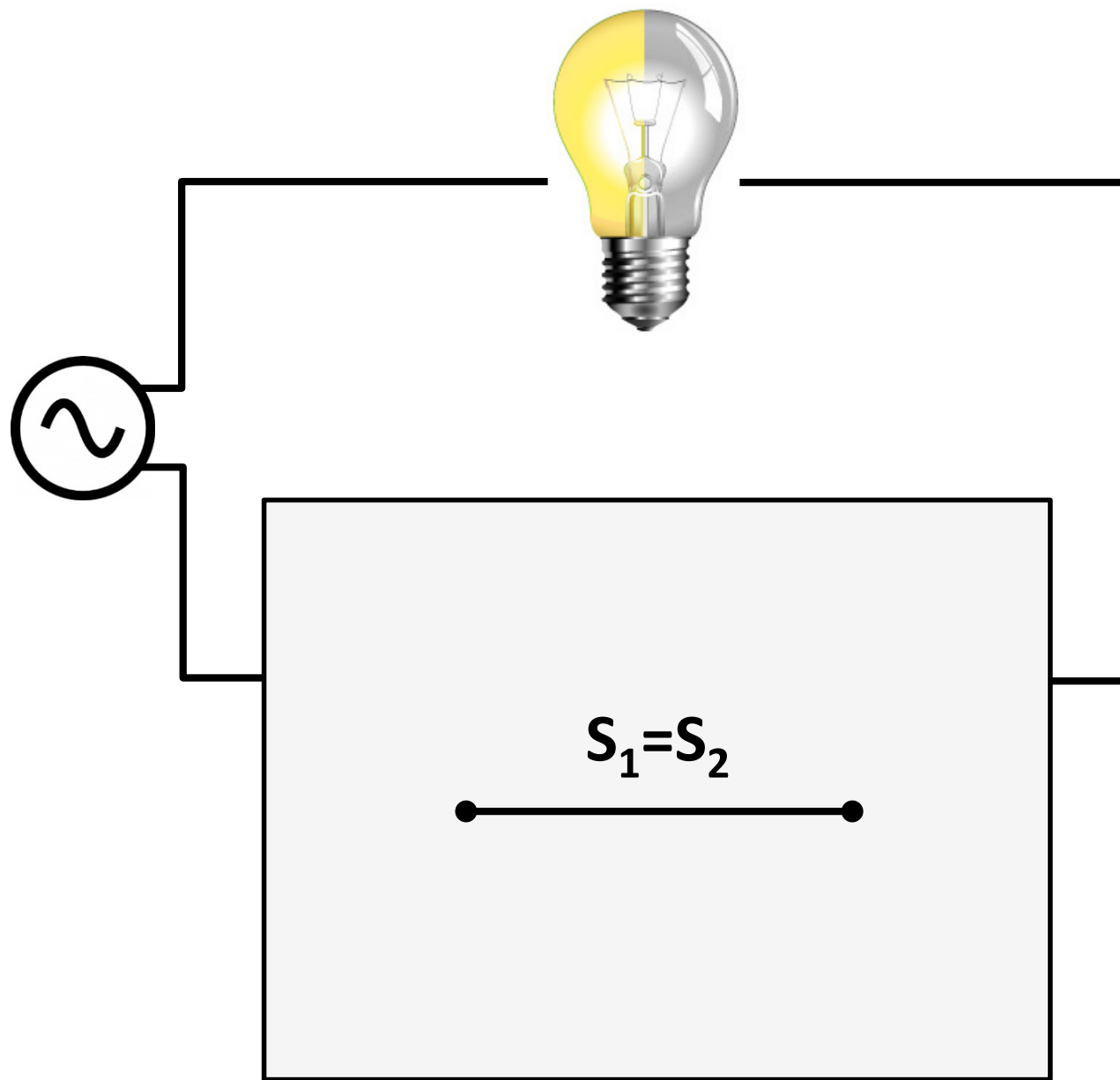






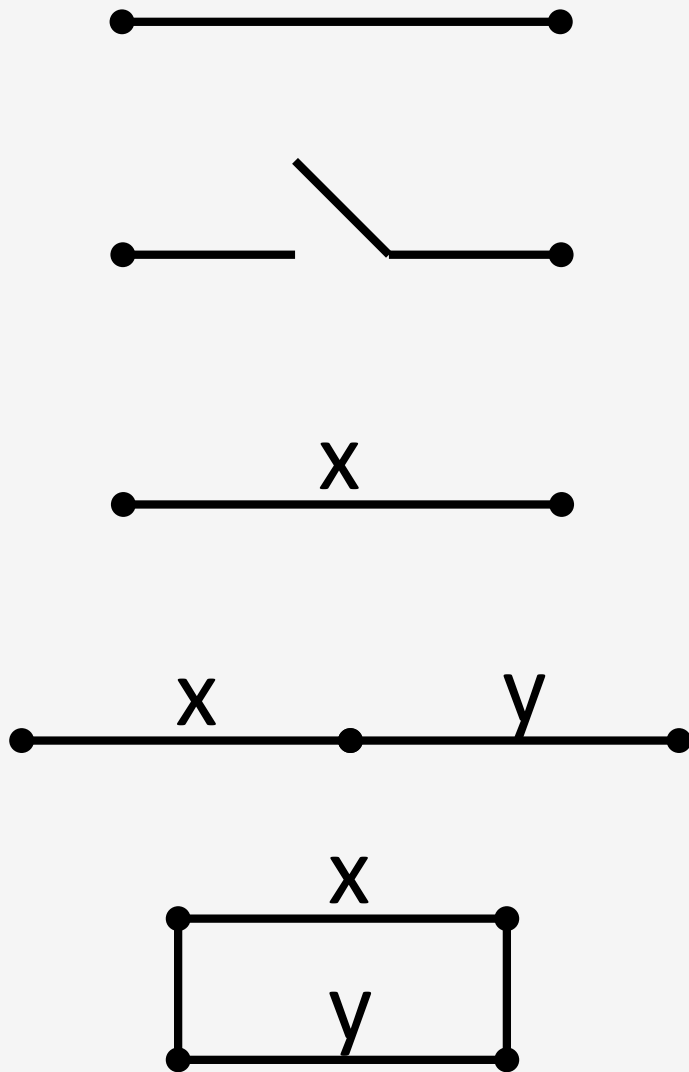






Shannon's Boolean analysis (1937)

Graph theory



$$f = 1$$

$$f = 0$$

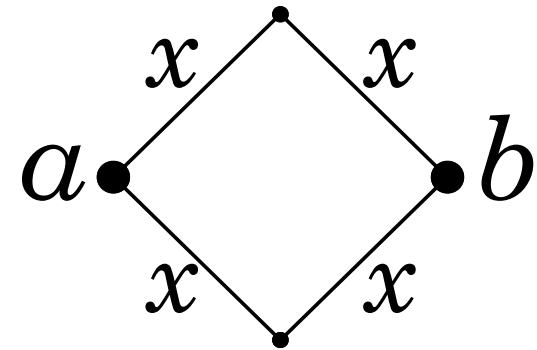
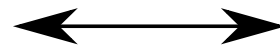
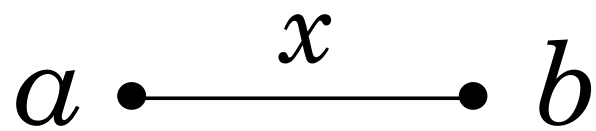
$$f = x$$

$$f = x \wedge y$$

$$f = x \vee y$$

Boolean algebra

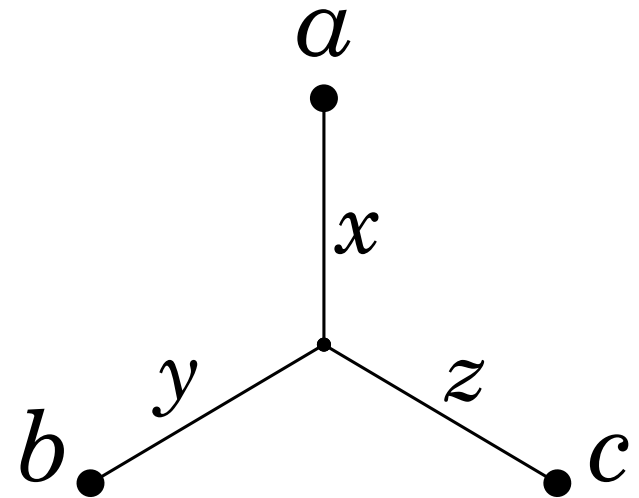
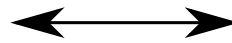
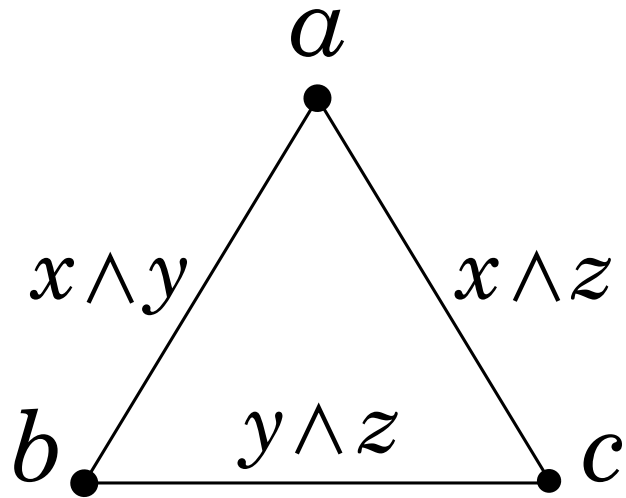
Equivalent transformations



$$f_{ab} = x$$

$$f_{ab} = (x \wedge x) \vee (x \wedge x) = x$$

Equivalent transformations



$$f_{ab} = x \wedge y$$

$$f_{ac} = x \wedge z$$

$$f_{bc} = y \wedge z$$

Part III: Algebra

“Algebra is arithmetic for lazy people.”

Author unknown

Algebra is arithmetic for lazy people



$$1 + 2 + 3 + \dots + 100 = ?$$

Algebra is arithmetic for lazy people

$$1 + 2 + 3 + \dots + 100 = ?$$

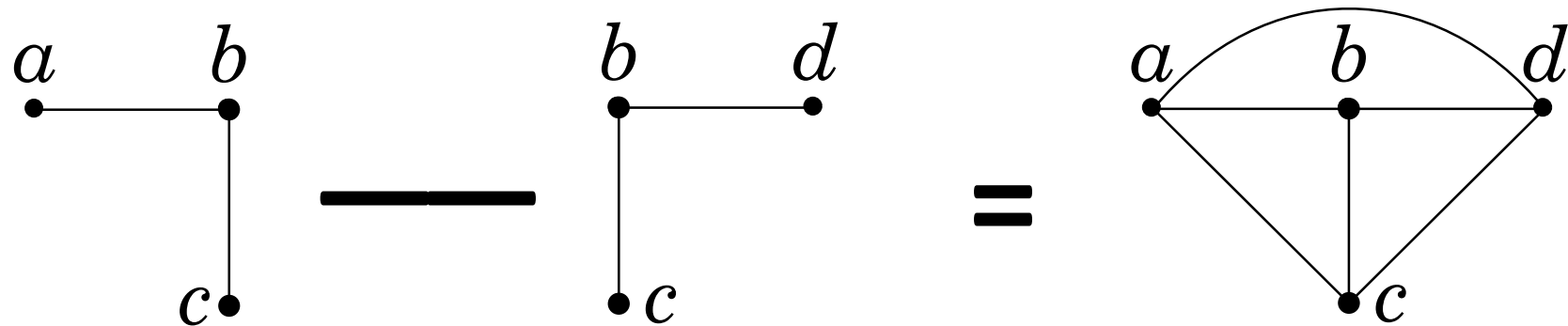
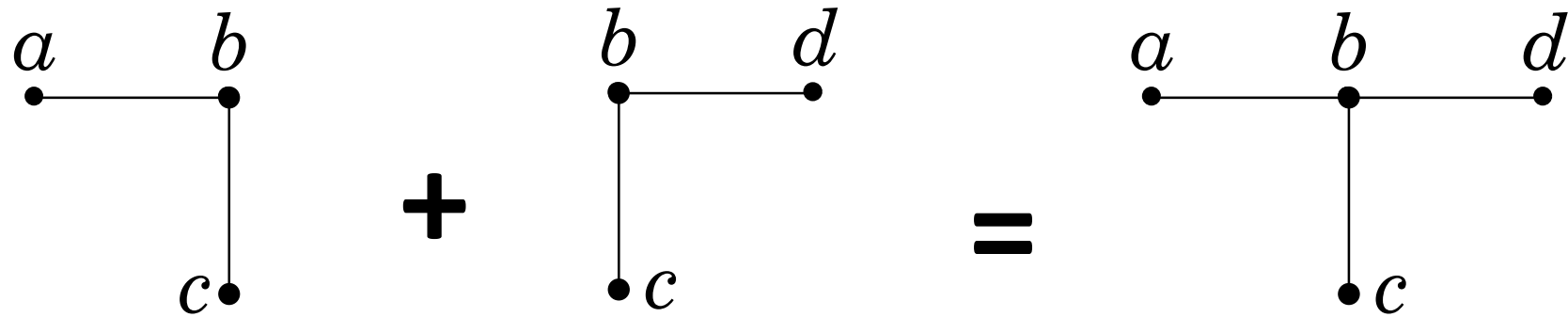
$$= (1 + 100) + (2 + 99) + \dots$$

$$= 101 + 101 + \dots$$

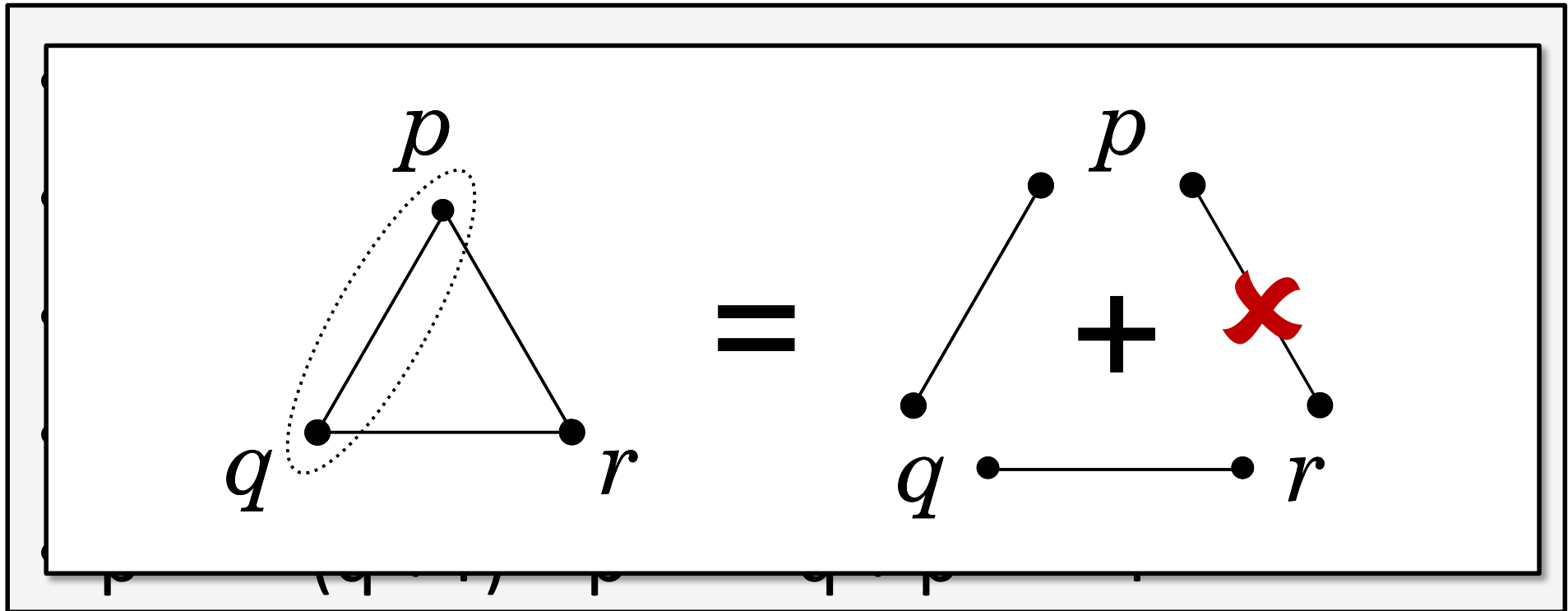
$$= 101 * 50$$

$$= 5050$$

Algebra of Switching Networks



Axioms



- $(p \text{ --- } q) \text{ --- } r = p \text{ --- } q + p \text{ --- } r + q \text{ --- } r$
- $(q \neq \varepsilon) \Rightarrow (p \text{ --- } q) \text{ --- } r = p \text{ --- } q + q \text{ --- } r$

Theorems

- $(p \text{ --- } q) \text{ --- } r = p \text{ --- } (q \text{ --- } r)$
- $p + \varepsilon = p$
- $p + p = p$
- $p + p \text{ --- } q = p \text{ --- } q$

Very different from arithmetic!

From graphs to families of graphs

- $[0]_p = \varepsilon$
- $[1]_p = p$
- $[x]_p$ is a family of two graphs: $\{\varepsilon, p\}$
- Switch is a family $\{p + q, p \text{ --- } q\}$
- $p \overset{x}{\text{---}} q = p + q + [x](p \text{ --- } q)$

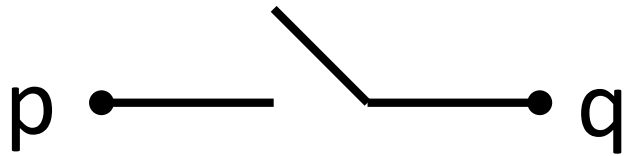
From graphs to families of graphs

- $[0]_p = \varepsilon$
- $[1]_p = p$
- $[x]_\varepsilon = \varepsilon$
- $[x]_{(p + q)} = [x]_p + [x]_q$
- $[x]_{(p - q)} = [x]_p - [x]_q$
- $[x \wedge y]_p = [x]_p [y]_p$
- $[x \vee y]_p = [x]_p + [y]_p$

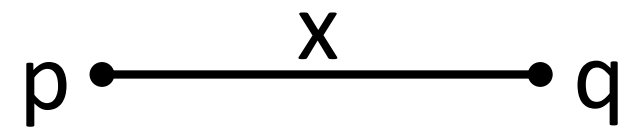
Algebraic representation



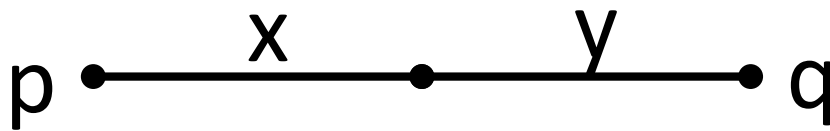
$$p \text{ --- } q$$



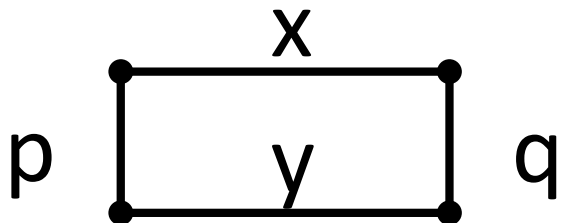
$$p + q$$



$$p \xrightarrow{x} q$$

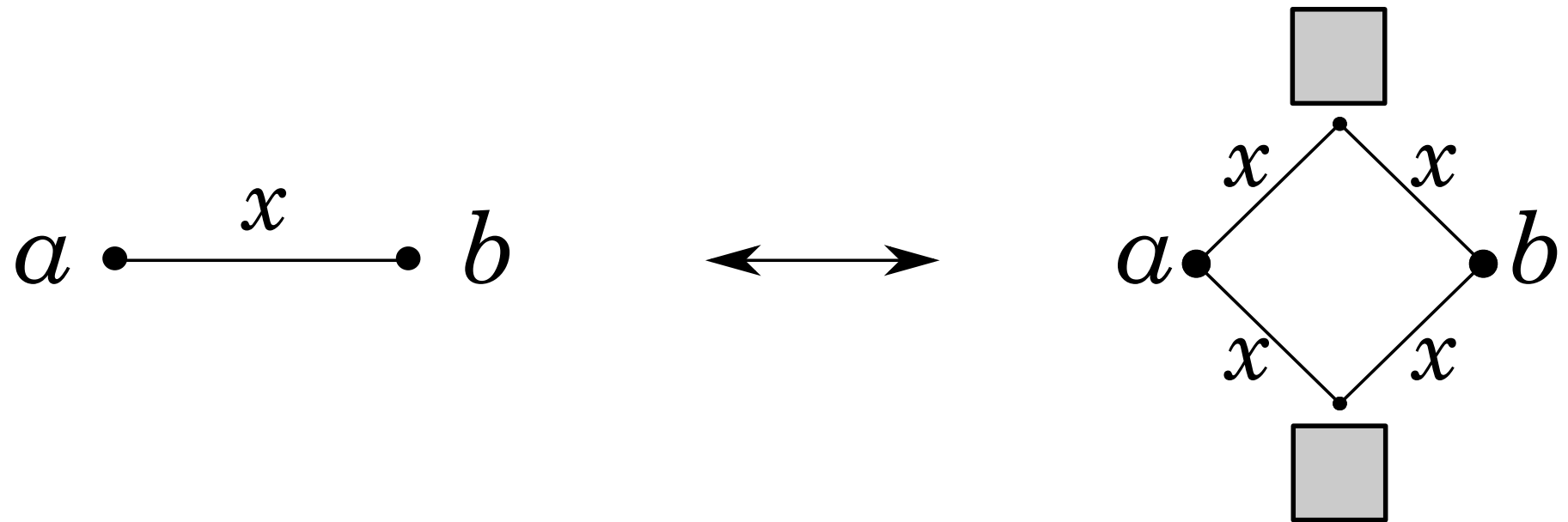


$$p \xrightarrow{x \wedge y} q$$



$$p \xrightarrow{x \vee y} q$$

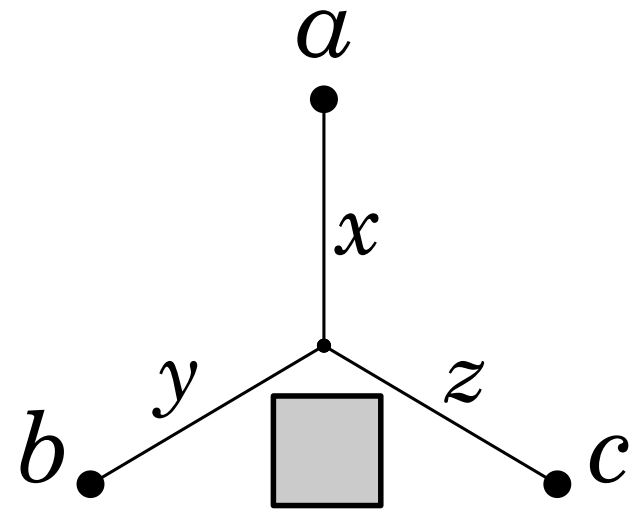
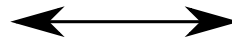
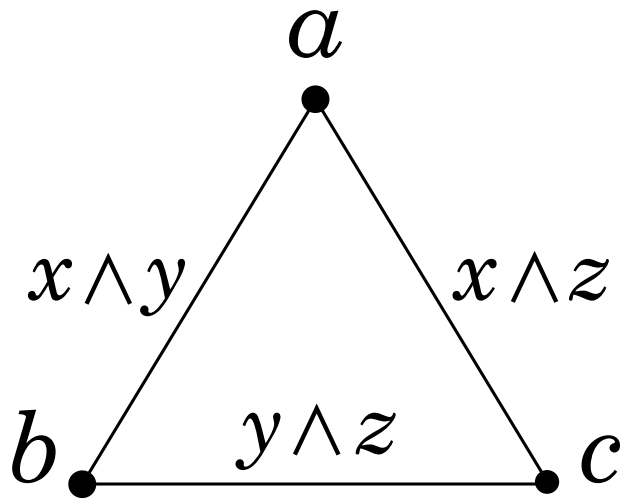
Equivalent transformations



$$a \xrightarrow{x} b = (a + b) \xrightarrow{x} (t_1 + t_2)$$

$\{t_1, t_2\}$

Equivalent transformations

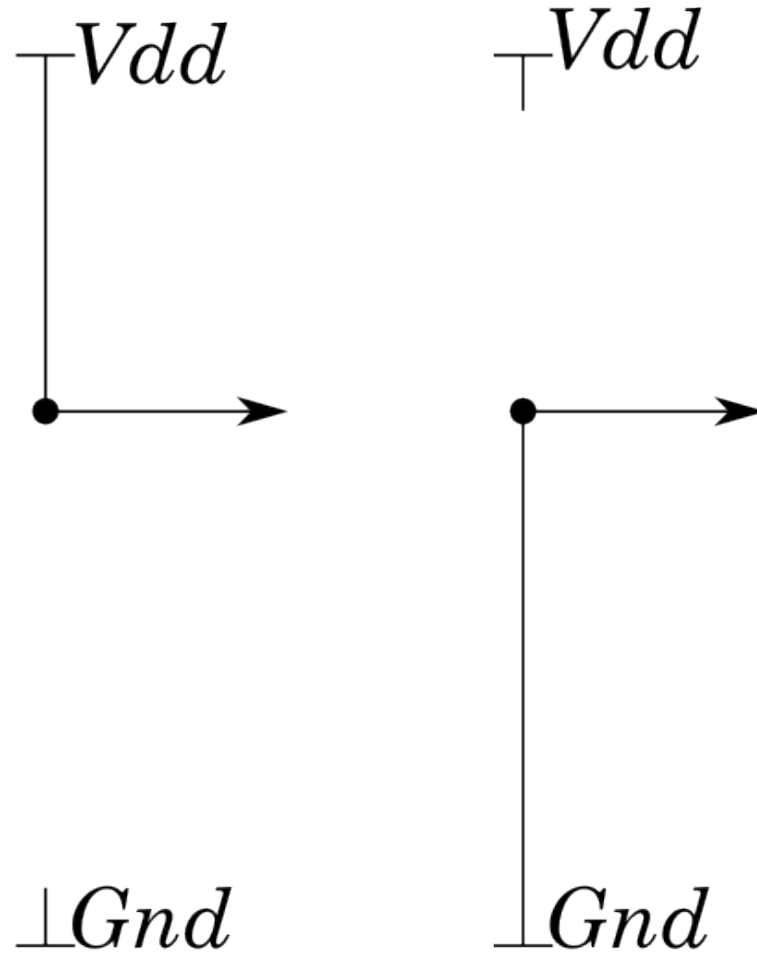


$$\begin{array}{l}
 a \frac{x \wedge y}{b} + \\
 a \frac{x \wedge z}{c} + \\
 b \frac{y \wedge z}{c}
 \end{array}$$

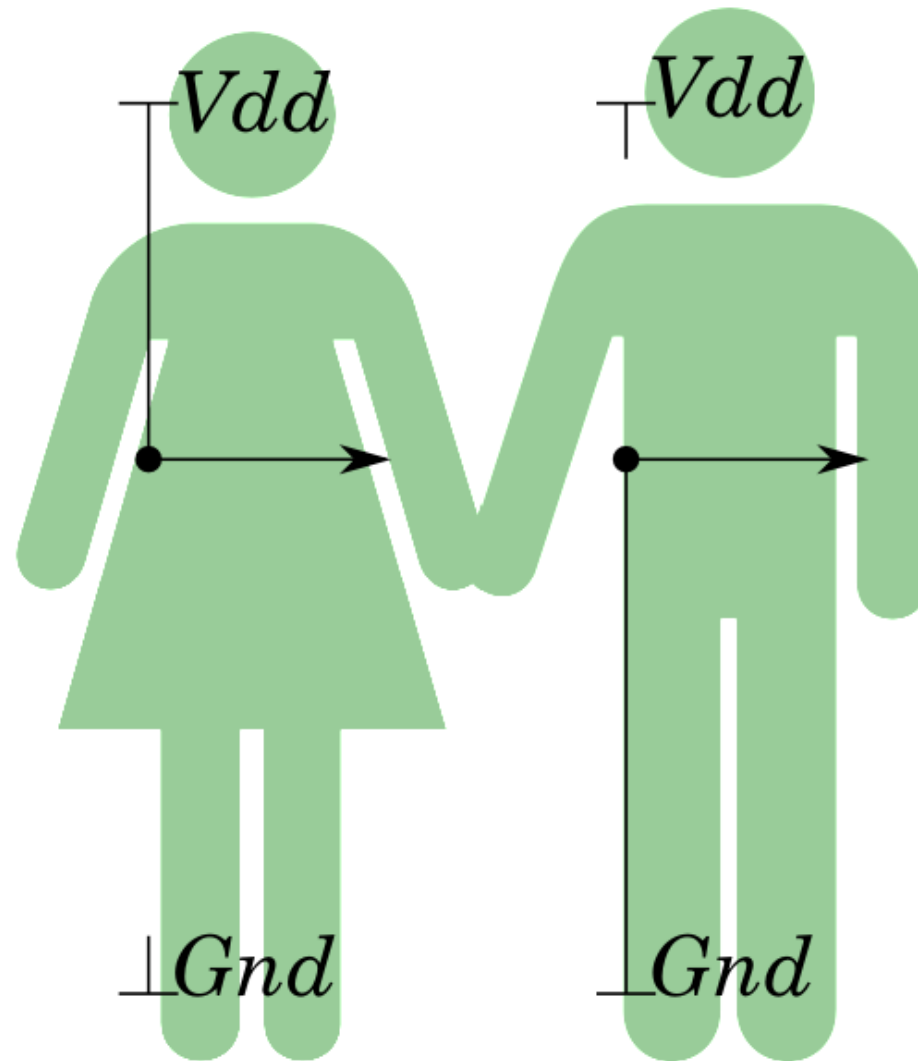
=

$$\begin{array}{l}
 a \frac{x}{t} + \\
 b \frac{y}{t} + \quad \backslash t \\
 c \frac{z}{t}
 \end{array}$$

CMOS family of networks

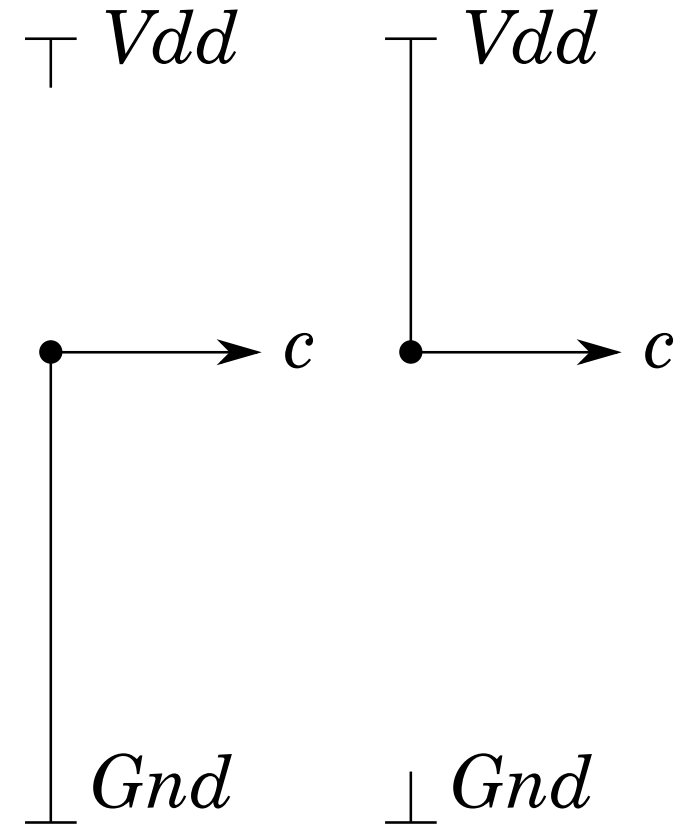


CMOS family of networks



NAND gate synthesis

$$\left\{ \begin{array}{l} \mathbf{X} = \top + c \text{ — } \perp, \text{ if } a \wedge b \\ \mathbf{X} = \top \text{ — } c + \perp, \text{ if } \overline{a \wedge b} \end{array} \right.$$

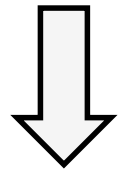


NAND gate synthesis

$$A = B, \text{ if } F \quad \Leftrightarrow \quad [F]A = [F]B$$

NAND gate synthesis

$$\left\{ \begin{array}{l} \mathbf{x} = \top + c \text{ — } \perp, \text{ if } a \wedge b \\ \mathbf{x} = \top \text{ — } c + \perp, \text{ if } \overline{a \wedge b} \end{array} \right.$$



$$\left\{ \begin{array}{l} [a \wedge b] \mathbf{x} = [a \wedge b] (\top + c \text{ — } \perp) \\ \overline{[a \wedge b]} \mathbf{x} = \overline{[a \wedge b]} (\top \text{ — } c + \perp) \end{array} \right.$$

NAND gate synthesis

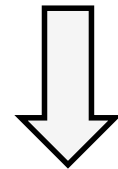
$$\left\{ \begin{array}{l} [a \wedge b]X = [a \wedge b](\top + c \text{ — } \perp) \\ \overline{[a \wedge b]X} = \overline{[a \wedge b]}(\top \text{ — } c + \perp) \end{array} \right. +$$

 by congruence

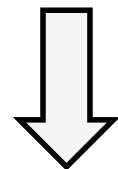
$$[a \wedge b]X + \overline{[a \wedge b]X} = [a \wedge b](\top + c \text{ — } \perp) + \overline{[a \wedge b]}(\top \text{ — } c + \perp)$$

NAND gate synthesis

$$[a \wedge b]X + [a \overline{\wedge} b]X = [a \wedge b](\top + c \text{ — } \perp) + [a \overline{\wedge} b](\top \text{ — } c + \perp)$$

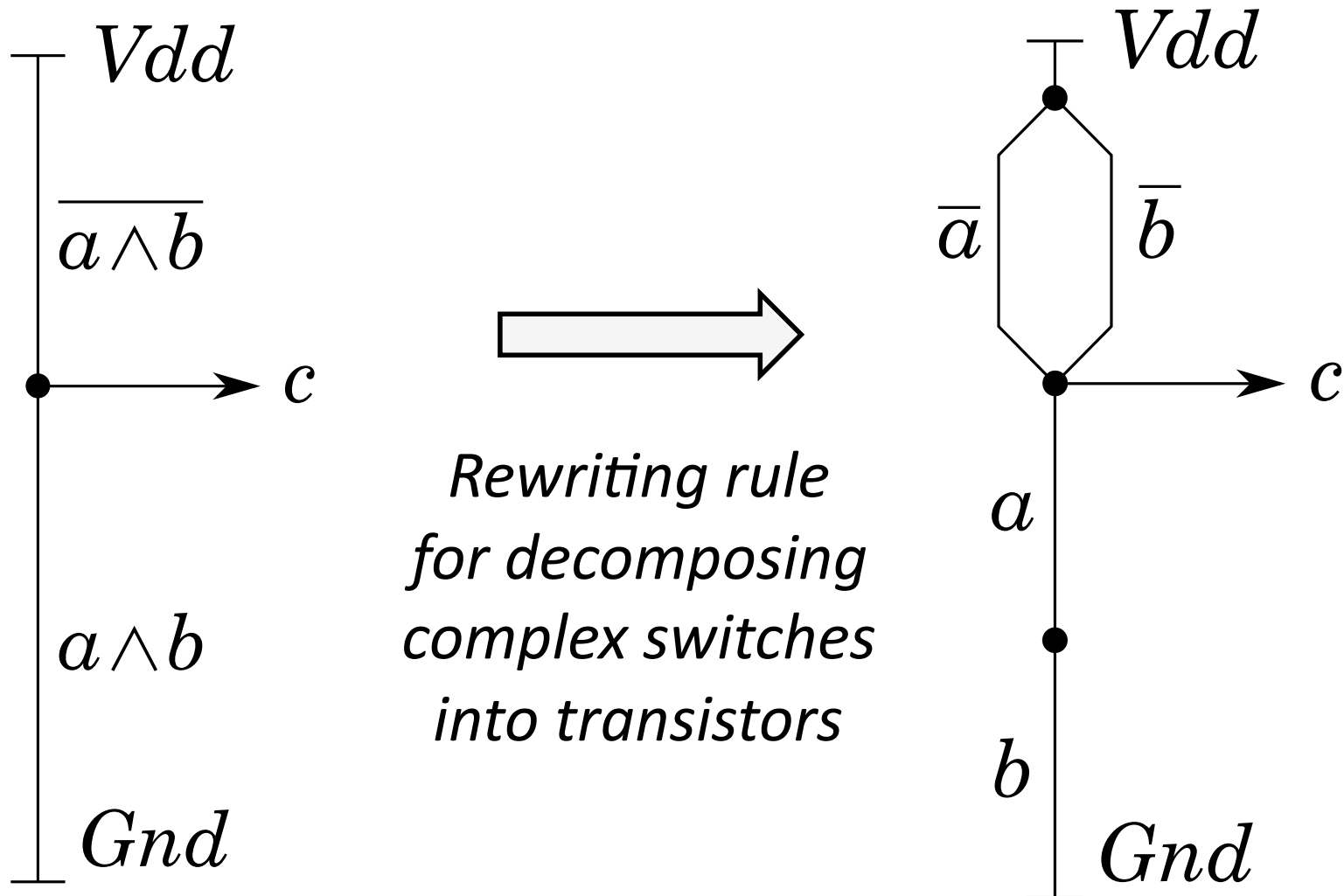
 factor

$$[(a \wedge b) \vee (a \overline{\wedge} b)]X = [a \wedge b](\top + c \text{ — } \perp) + [a \overline{\wedge} b](\top \text{ — } c + \perp)$$

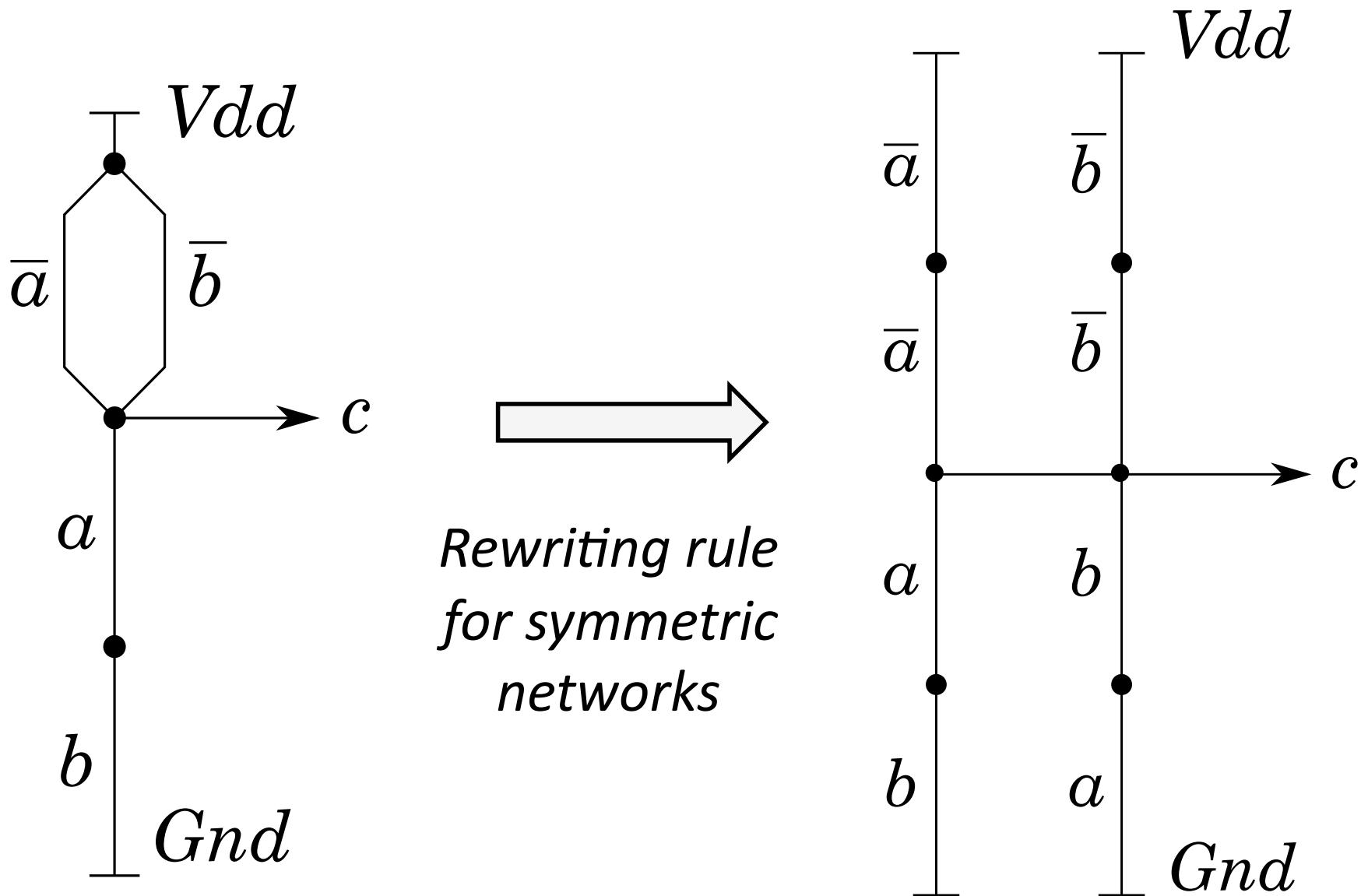
 simplify

$$X = [a \wedge b](\top + c \text{ — } \perp) + [a \overline{\wedge} b](\top \text{ — } c + \perp)$$

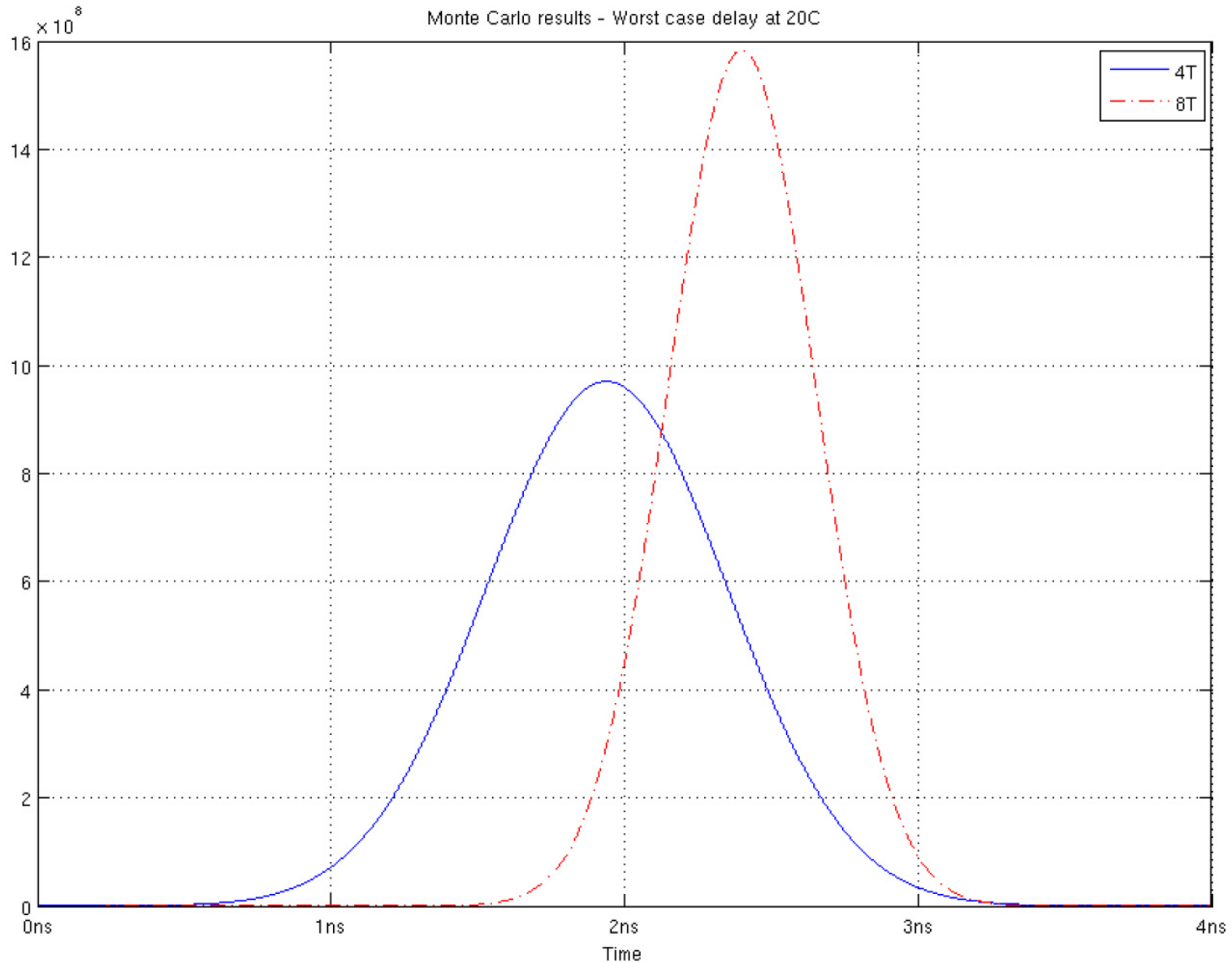
NAND gate synthesis



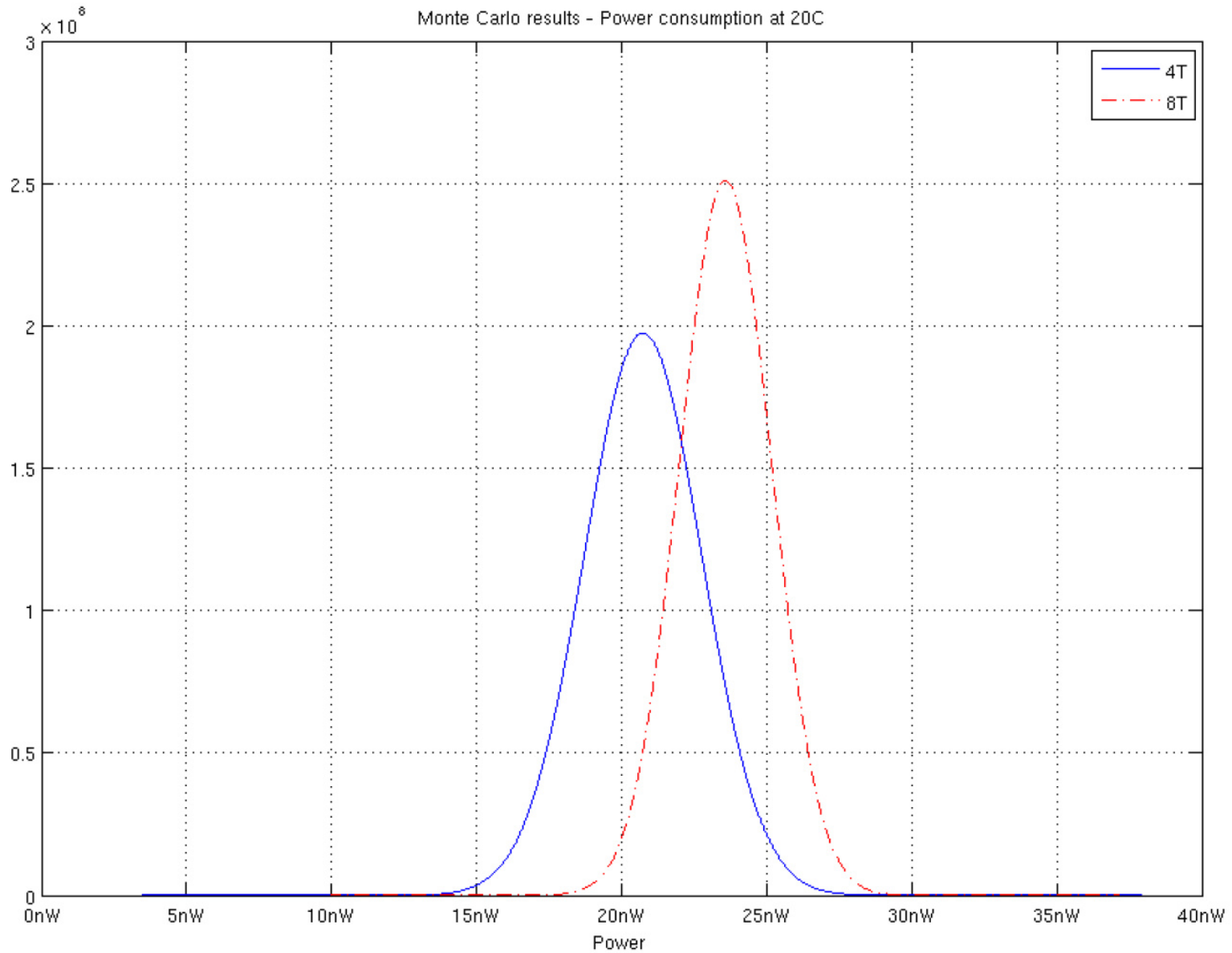
Decreasing uncertainty



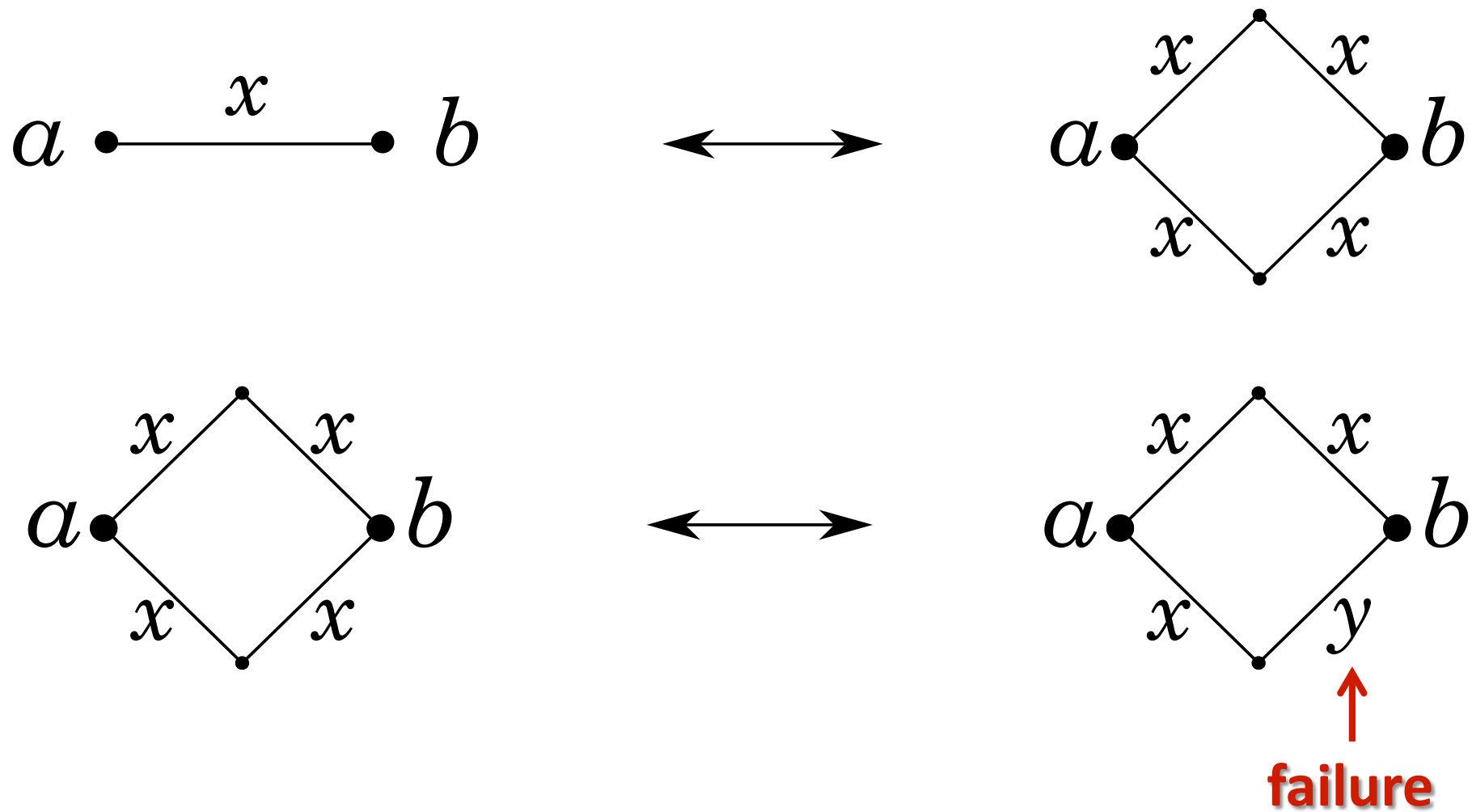
Decreasing uncertainty (delay)



Decreasing uncertainty (power)



Checking non-functional properties



Thank you!