New Reliable Reconfigurable FPGA Architecture for Safety and Mission Critical Applications

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ARDyT

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Introduction

Design Flexibility

High Density Functionality

High Performance Computing

Reason to Move Towards

SRAM Based FPGAs

Applications such as,

Aero-Space

Nuclear

Medical

are

Prone to Radiation Induced, Single Event Effects (SBU, MBU, etc.,)

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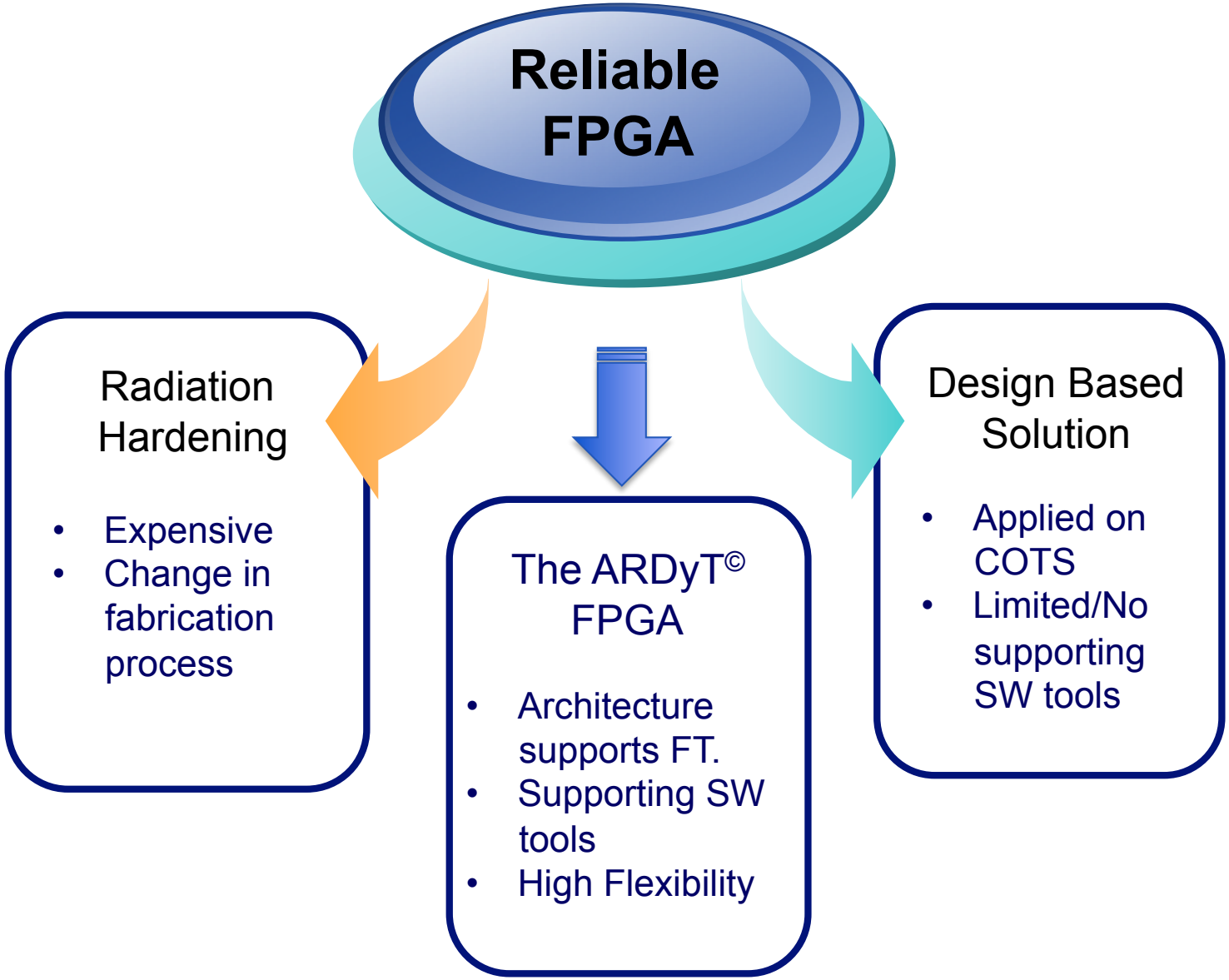
Making FPGA Architecture "Reliable"



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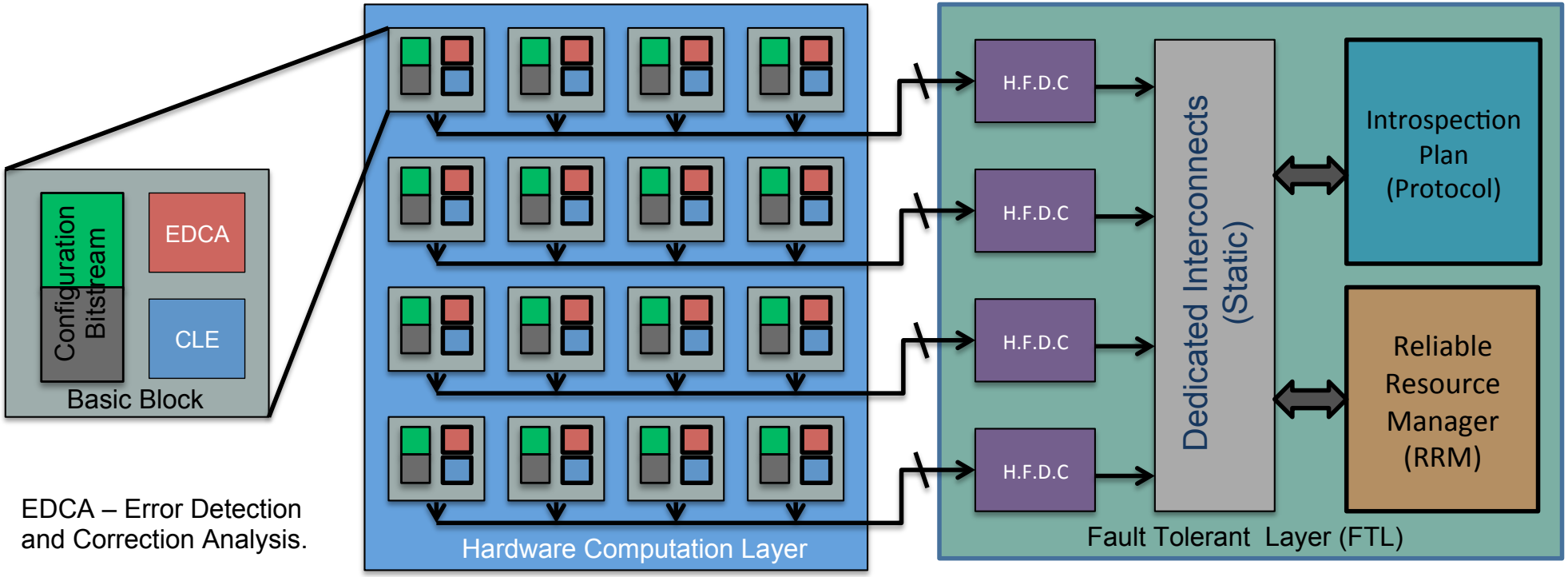
ARDyT© FPGA Architecture



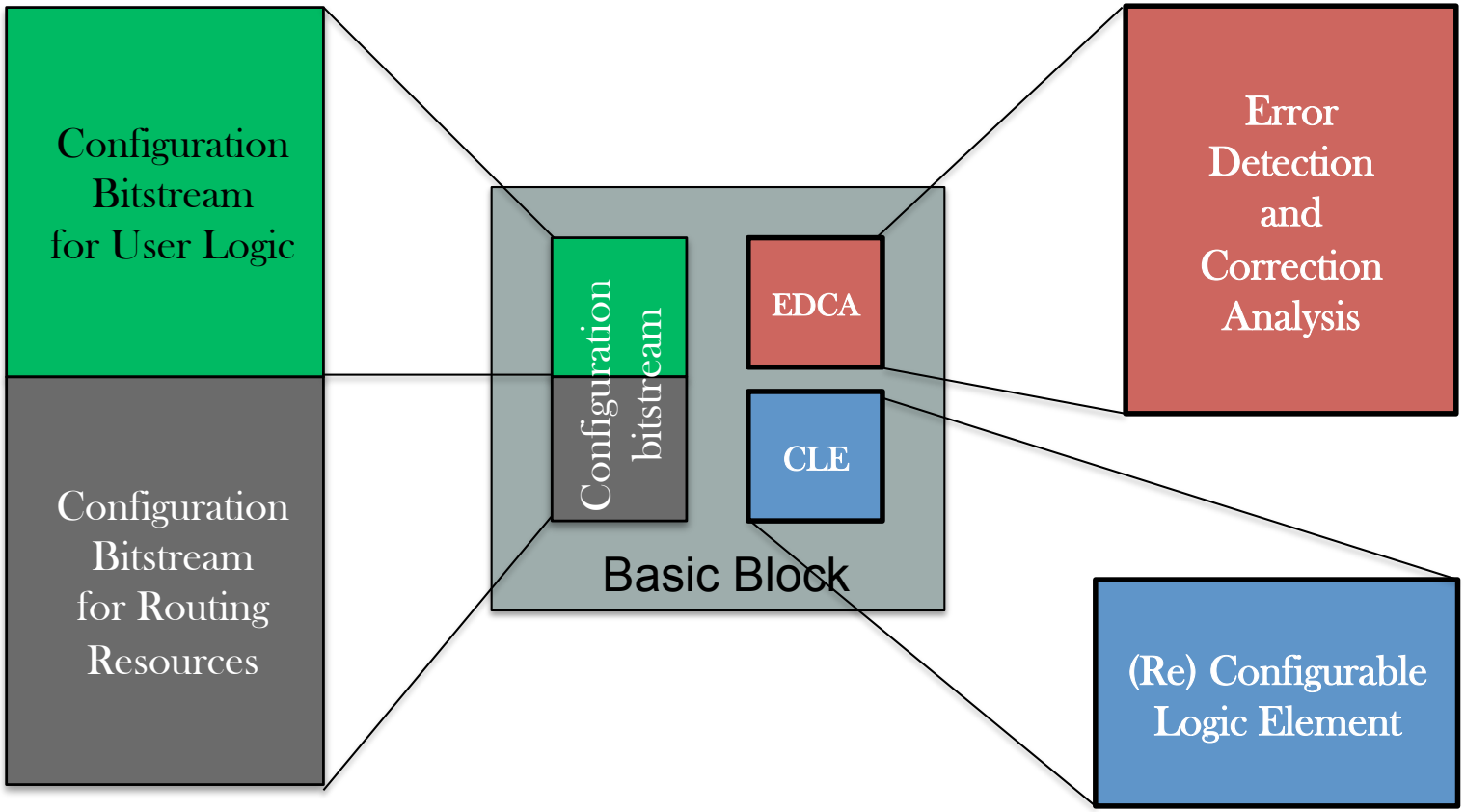
EDCA – Error Detection and Correction Analysis.

CLE – Configurable Logic Element.

Basic Building Block Cluster

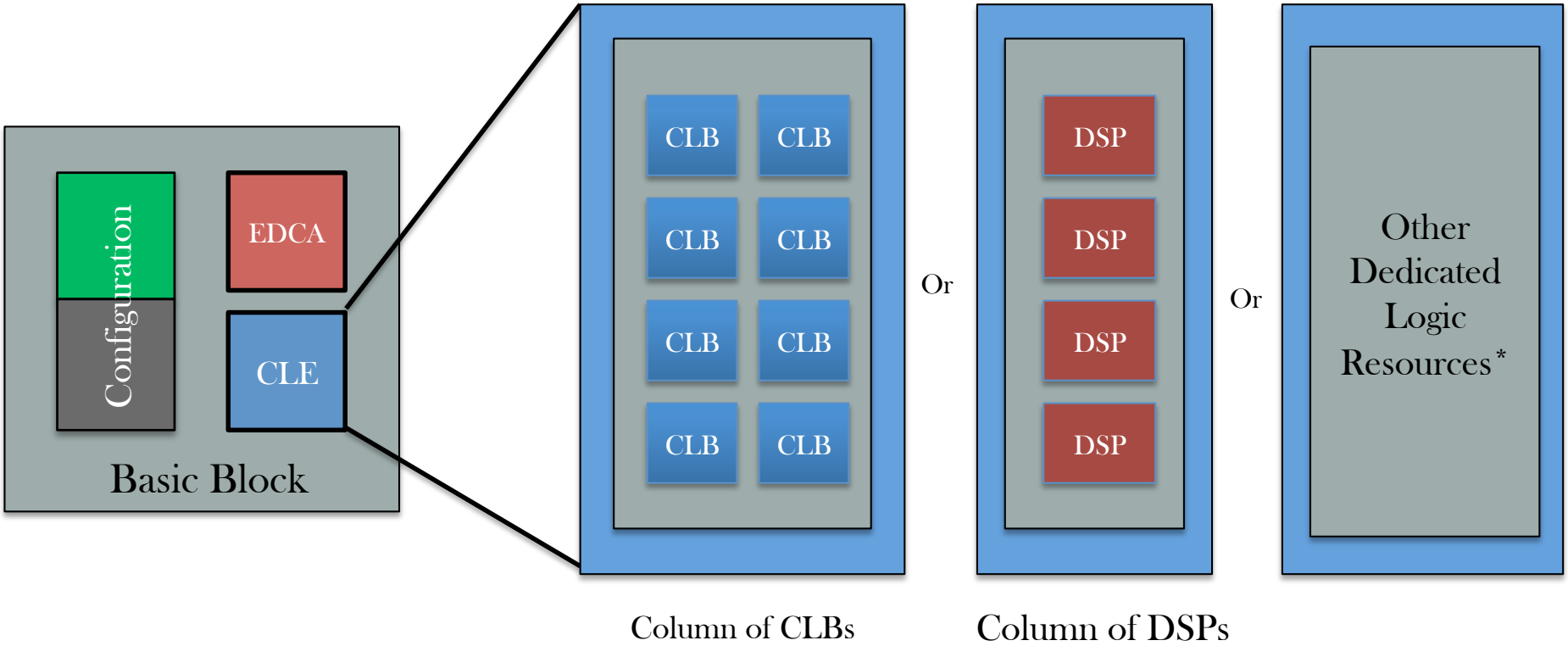
*H.F.D.C – Hierarchical Fault Detection Chain

Basic Building Block



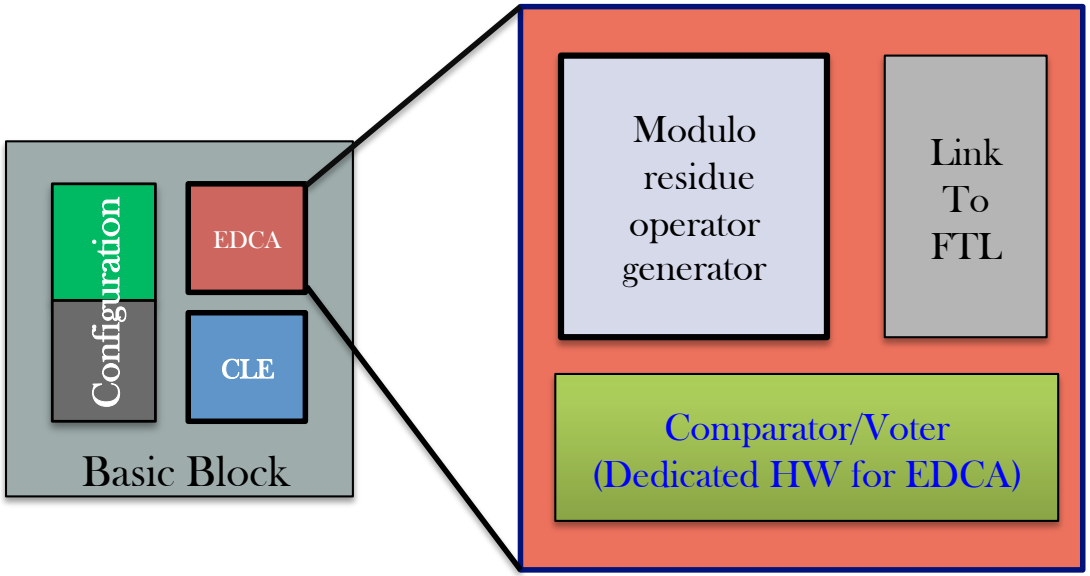
Configurable Logic Element

Logic elements of similar hardware size grouped to form a CLE.



* Of same hardware equivalance.

Error Detection and Correction Analysis



EDCA has dedicated hardware to perform the error detection on the Configurable Logic element of its own Basic block.

Provides link to the FTL; Primarily connected to H.F.D.C

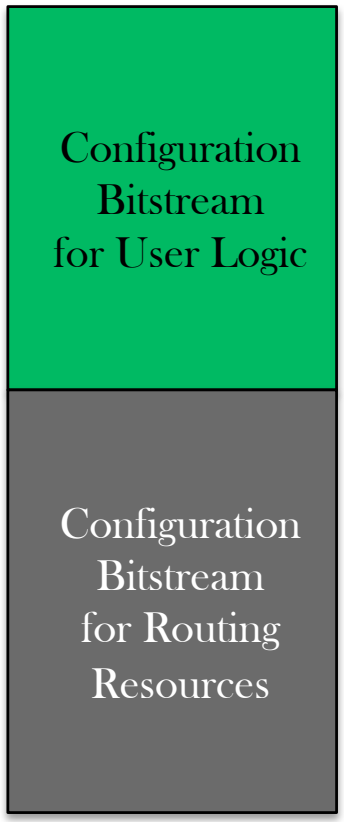
The dedicated fault detection hardware could be,

Simple 1. **Comparator** in case of Duplication/Dual Modulo Redundancy

2. A **voter** in case of Triple Modulo Redundancy

3. Modulo residue operator generator in case of Arithmetic Logic Unit etc.,

Dedicated Configuration Bitstream



- Identifying bitstream of a particular Basic Block. Identifying the exact error zone.
- Distinguishing bitstream corresponds to Logic Resources and Routing Resources
- Detailed fault identification at the required granularity level.
- The computational errors can be handled internally in the Basic Block. The routing errors can be handled by run time re-routing.
- Improves flexibility in fault mitigation.

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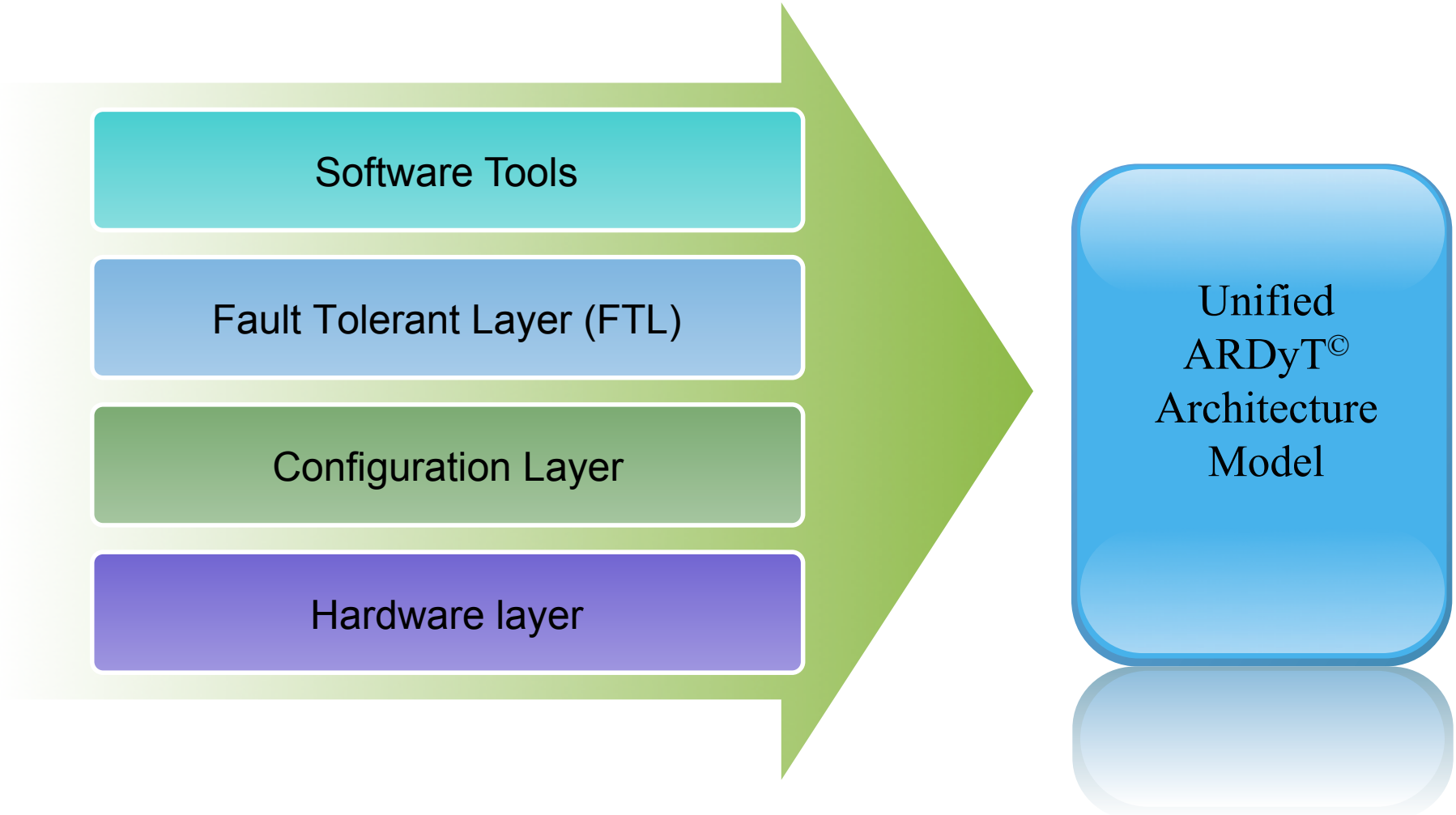
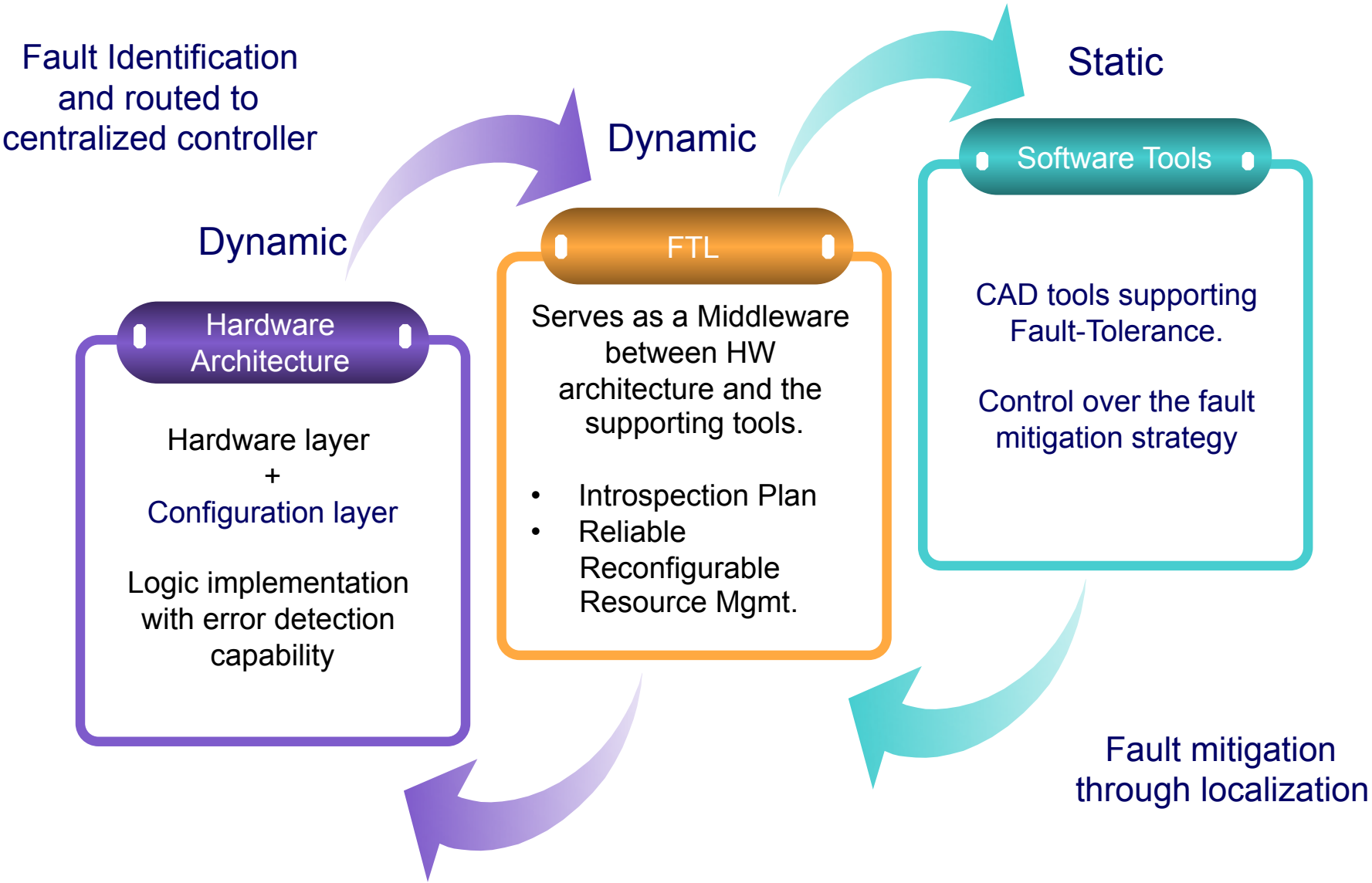
Fault Tolerant Layer (FTL)



FTL as Middleware

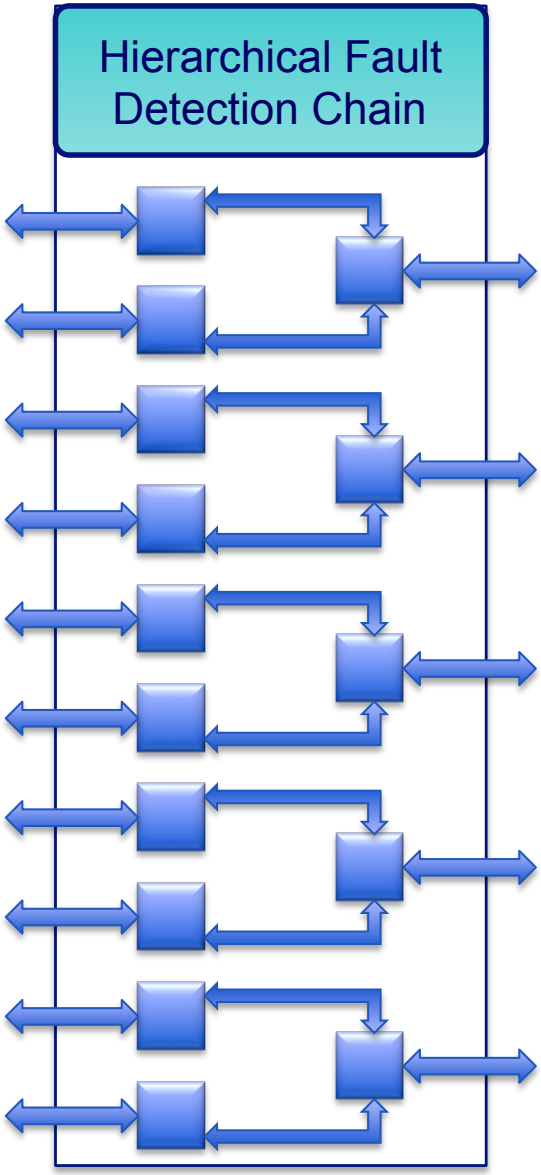


Introspection Plan

Hardware Architecture Side

Error detection signals from Basic blocks

Through 'Link to FTL' in EDCA



Fault Tolerant Layer Side

Interrogation Protocol

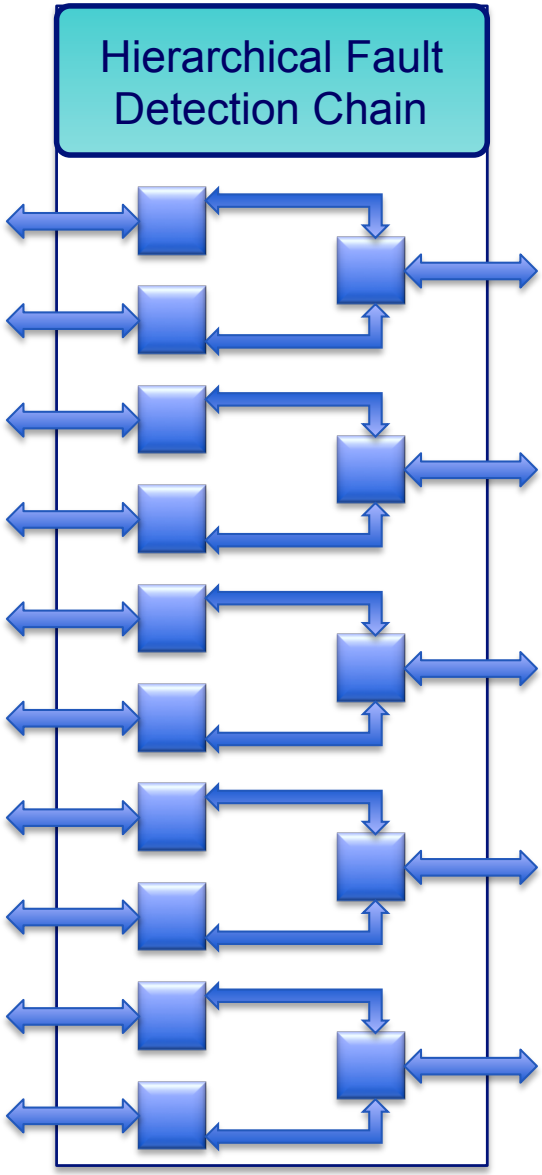
Polling

or

Interrupt Handling

- Reduction gate

Introspection Plan



Fault Tolerant Layer Side

Dedicated Interconnects (Static)

H.F.D.C is connected to FTL via static dedicated interconnects

Static resources occupy less hardware than dynamic one.

H.F.D.C discards the permanently faulty resources from FTL.

Reduced number of lines connected between hardware architecture and FTL.

- Reduction gate module

Reliable Resource Management

- Reliable Resource Manager (RRM), works together with Introspection plan

- The interrogation protocol interacts with EDCAs and provides input to the RRM. (via H.F.D.C and Static interconnects)

- Upon receiving information about the fault and its nature, RRM decides the action need to be taken.

- Trade-off :

Not all the resources in the FPGA have to be compulsorily protected.
{Hardware cost, Timing overhead, etc.,} Vs {Level of Reliability Provided}

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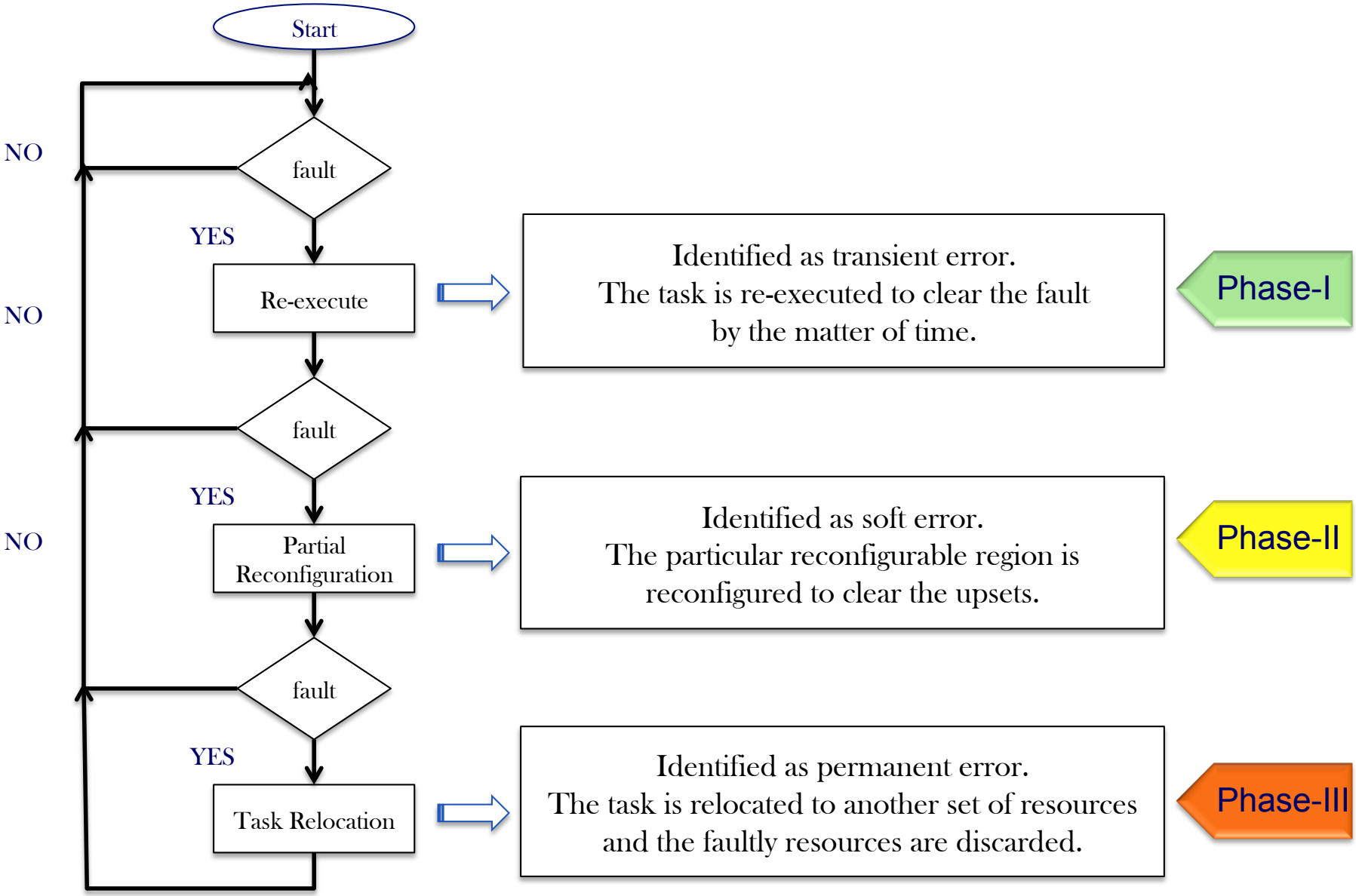
General Flow of Fault Mitigation



Novelty in Phase II

Recent experimental results on Xilinx Kintex7 FPGAs indicate,

9.9% events cause Multi-Bit Upsets (MBU) [1] MBU on every 1515s (about 25 mins)

Conventional solution,

Dynamic Partial Reconfiguration + Dedicated Golden Copy of the Configuration Bitstream

☹ Protecting the same amount of bitstream twice ☹

Proposed solution in ARDyT FPGA,

Dynamic Partial Reconfiguration + Built-in Hamming Code Based Multi-Bit Error Correction

[1] Helio Takai et al.,'Soft error rate estimations of the Kintex-7 FPGA within the ATLAS Liquid Argon (LAr) Calorimeter', in TWEPP'13, Italy, 23-27 Sept 2013.

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Supporting Tool Suite

- New architecture, without any supporting Computer Aided Design (CAD) tools, would be largely insufficient.

- ARDyT© provides complete design framework allowing designers to program and use this architecture.

The toolset offers,

Fast Modelling Capabilities	Virtual Prototyping Environment
As the architecture is subject to change during the exploration phase	CAD software to validate a design before making a physical prototype

Biniou: ARDyT© Modelling

Biniou, a software tool, offers the embryologic version of the proposed ARDyT© model.

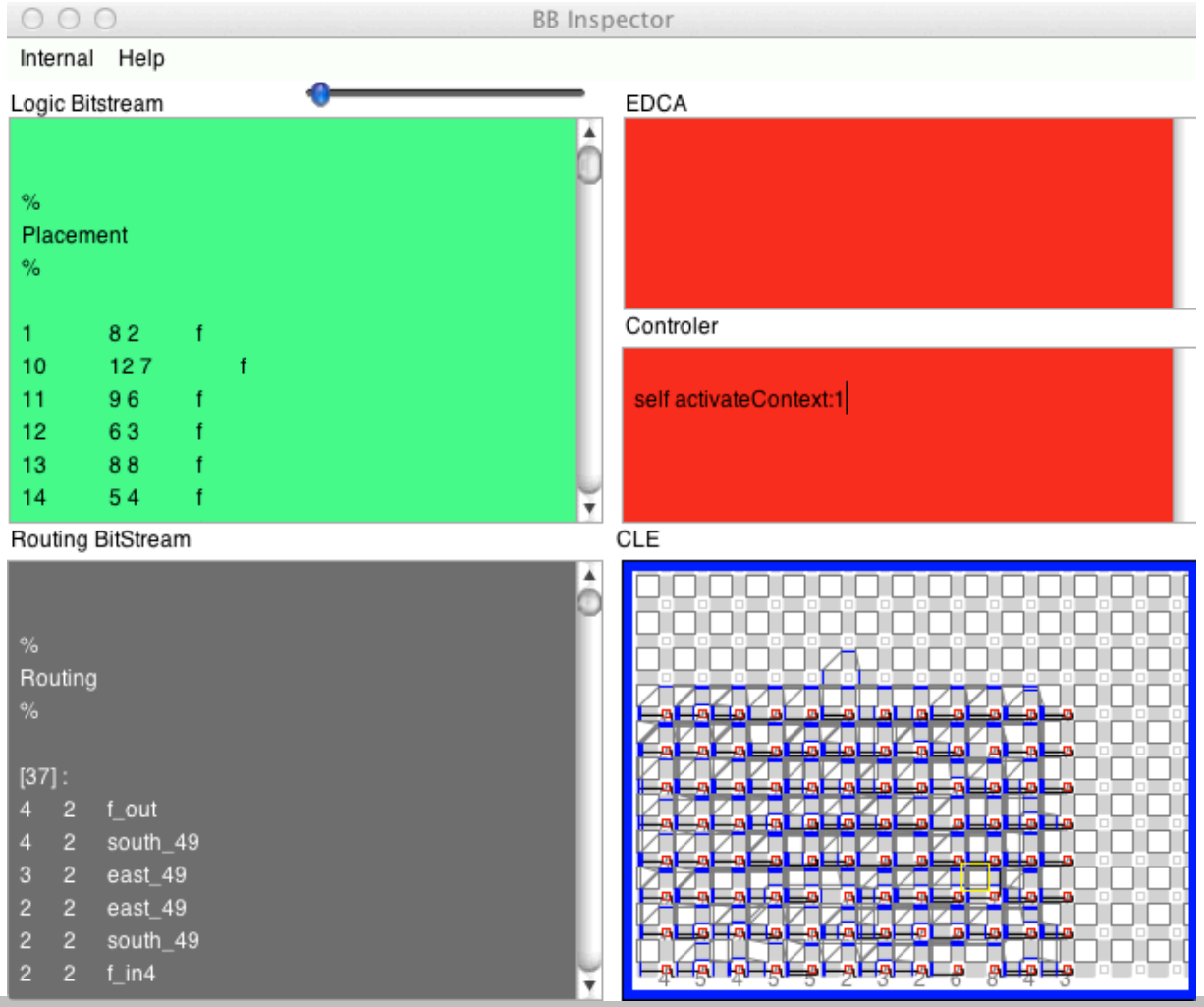

Figure : From concept to toolset by resuing and tailoring existing software environment, Biniou.

It illustrates, the reuse of Biniou, as a system analysis tool and shows configured basic block (bottom right) with programmable controller (top right) and textual representation of bitstream (left).

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Conclusion/Prospective Plan

New low-cost fault-tolerant FPGA architecture is proposed to facilitate the mission critical applications.

Novelty of the architecture: Dedicated fault mitigation resources added locally to the Basic blocks and it's interface to the specially consecrated fault-tolerant layer.

Newly added features provide increased flexibility in the architecture to attain required level of reliability without depending on full radiation hardening.

Now the focus is on handling task relocation (upon permanent error) and task synchronization (after partial reconfiguration).

Acknowledgement

The work presented here is a integral party of ARDyT project

In collabration with,

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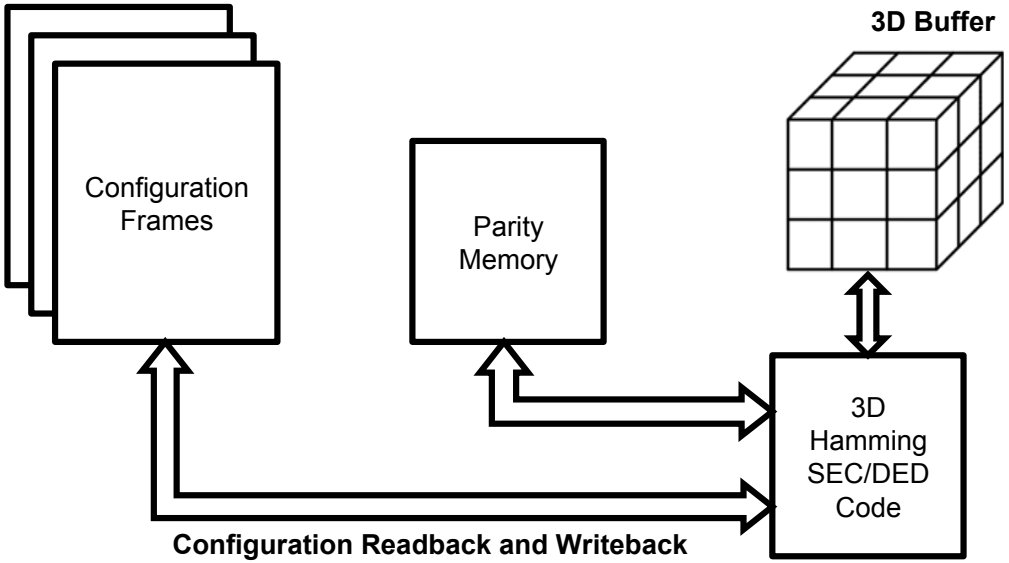
iD4CAR images & réseaux support.

Thank You !

ARDyT

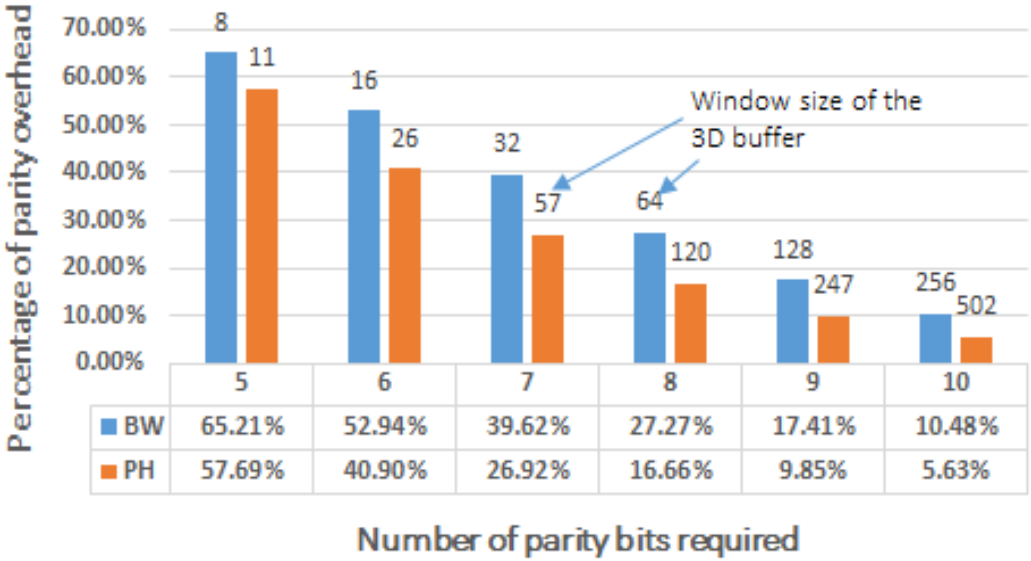
Built-in 3D-Hamming EC Scheme



Reference : Chagun Basha, Sébastien Pillement and Stainslaw Piestrak, 'Built-in 3-Dimentional Hamming Multiple-Error Correcting Scheme to Mitigate Radiation Effects in SRAM-Based FPGAs', ARC'14 April 2014, Portugal.

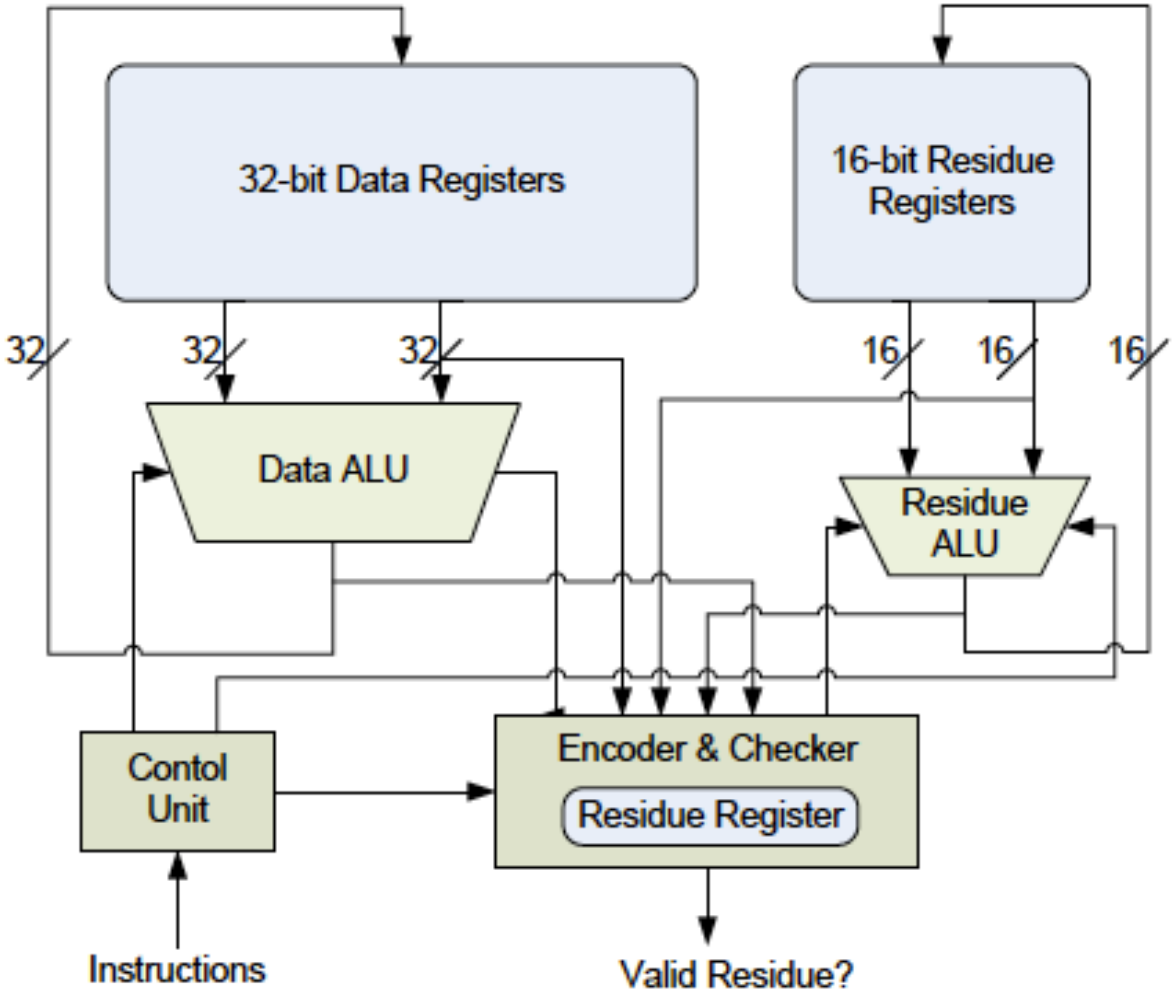
- Built-in protection
- Less parity memory overhead
- Improved Multiple bit error correcting capability.

Optimization of Parity Memory Overhead



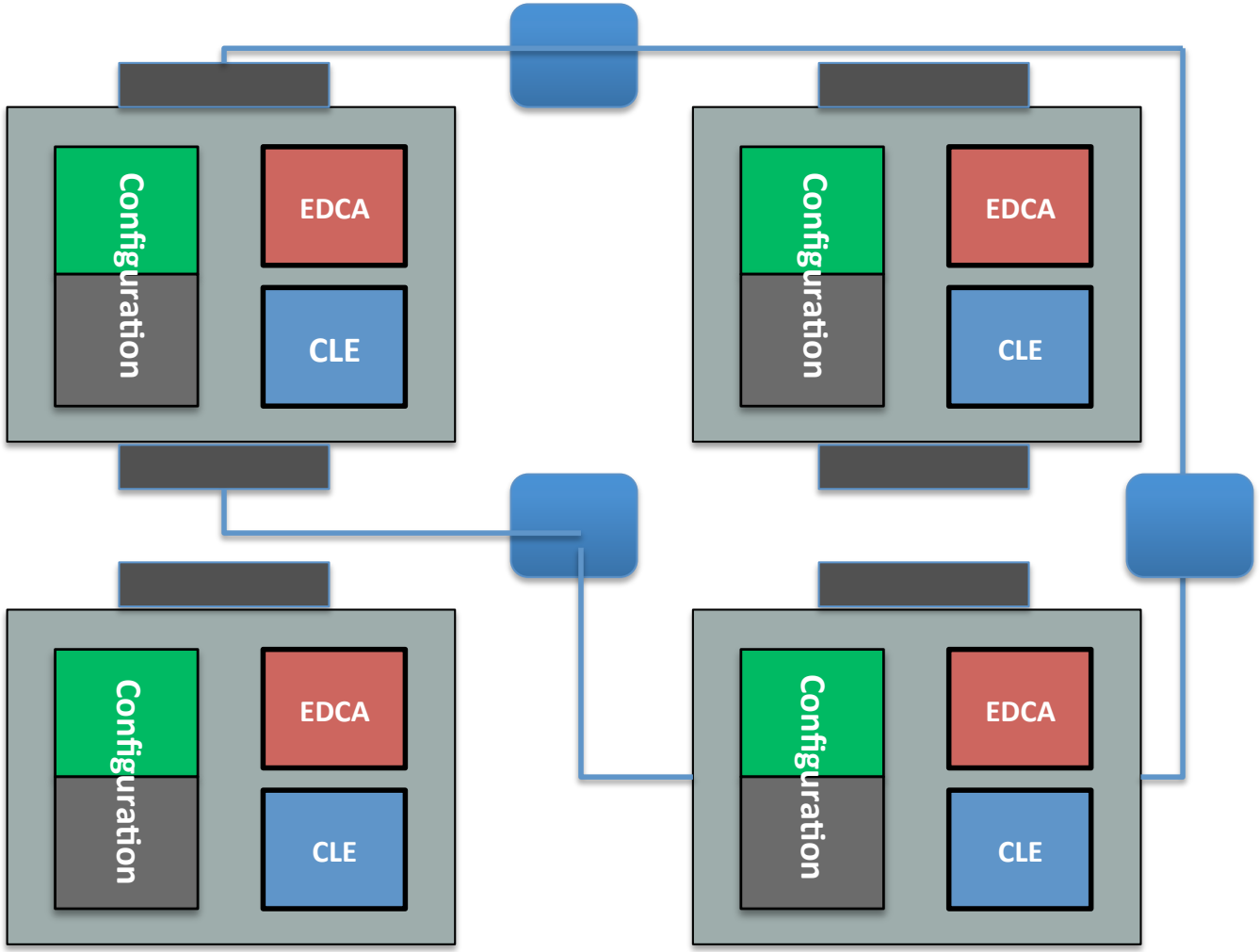
	5	6	7	8	9	10
BW	65.21%	52.94%	39.62%	27.27%	17.41%	10.48%
PH	57.69%	40.90%	26.92%	16.66%	9.85%	5.63%

Modulo Residue Code for ALU protection



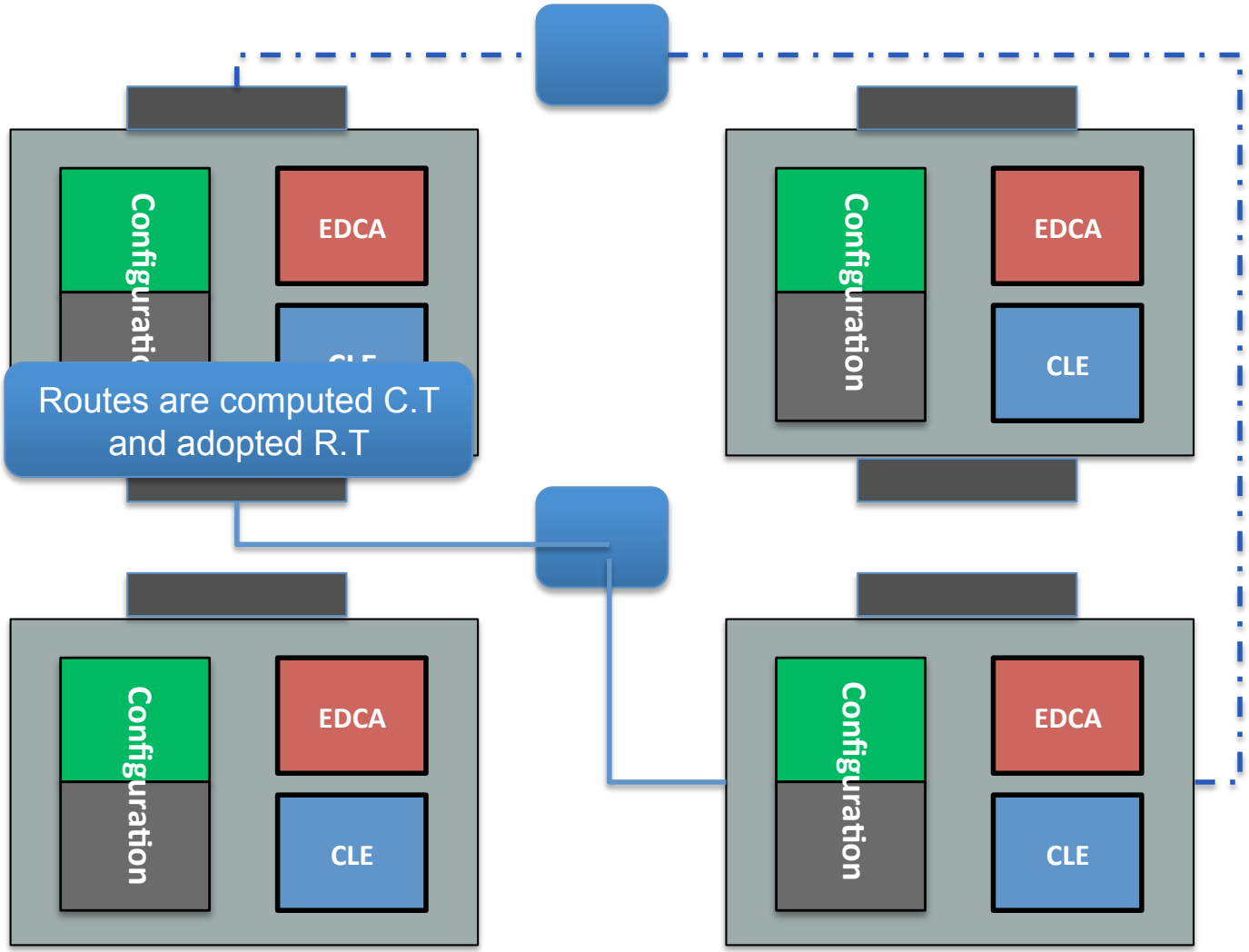
Reference: Marcel Medwed et al., 'Arithmetic Logic Units with High Error Detection Rates to Counteract Fault Attacks' DATE 2011.

Fault Mitigation in Routing Resources



Each signal is routed twice - physical route redundancy

Fault Mitigation in Routing Resources



Routes are computed Compile Time (C.T) and adopted Real Time (R.T)