MUSTARD: A CAD tool for Predicting the Impact of Random Telegraph Noise on SRAMs and DRAMs

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Joint work with

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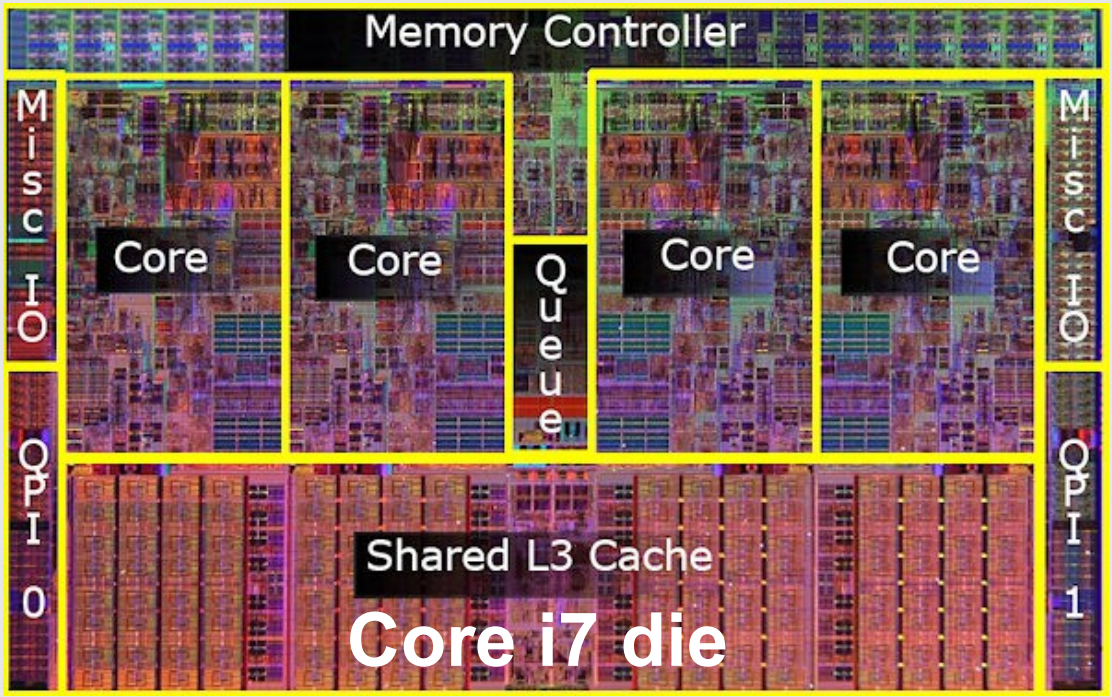
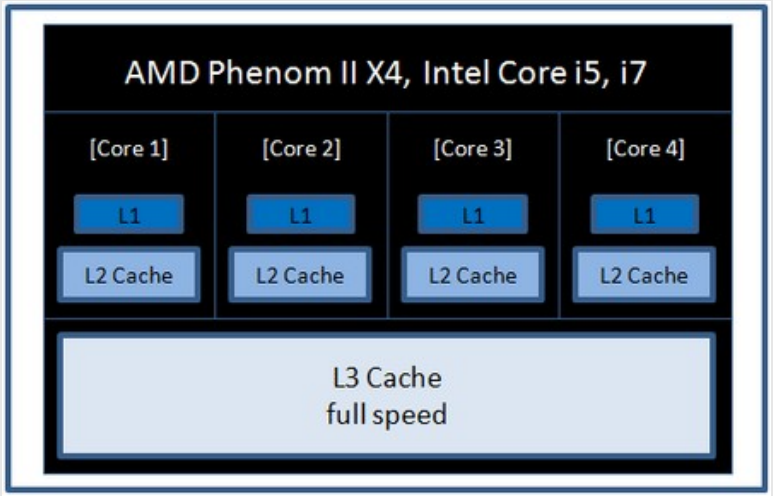
Overview of this talk

- **Why worry about RTN? (SRAMs, DRAMs)**
- **RTN basics**
- **Our contributions: RTN+circuit co-simulation**
  - discrete Monte-Carlo ↔ nonlinear ckt. simulation

Importance of SRAMs and DRAMs





Cache memory (L1, L2, L3, etc.)

↓

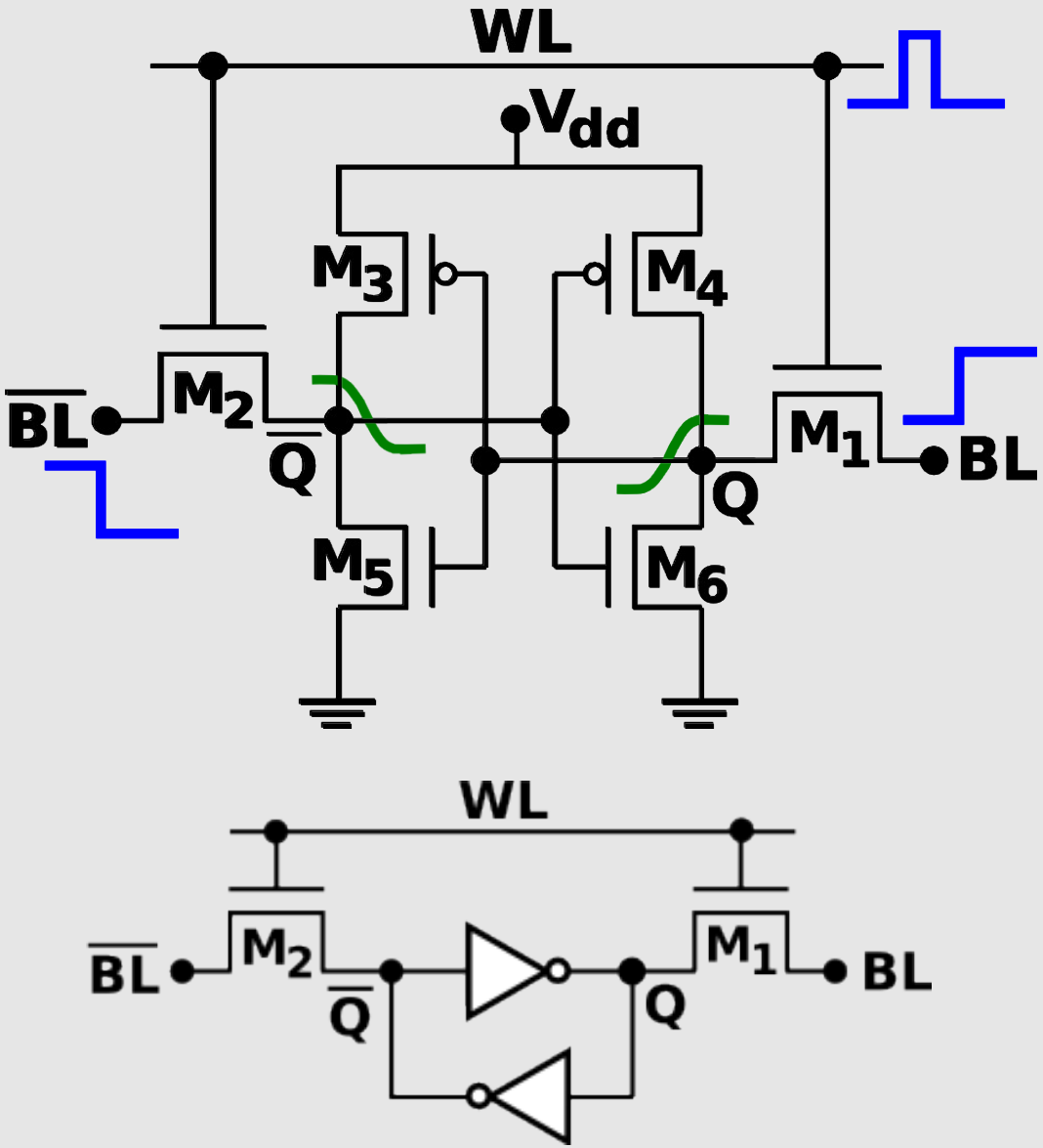
Millions of SRAM cells

Laptop, desktop, tablet memories

↓

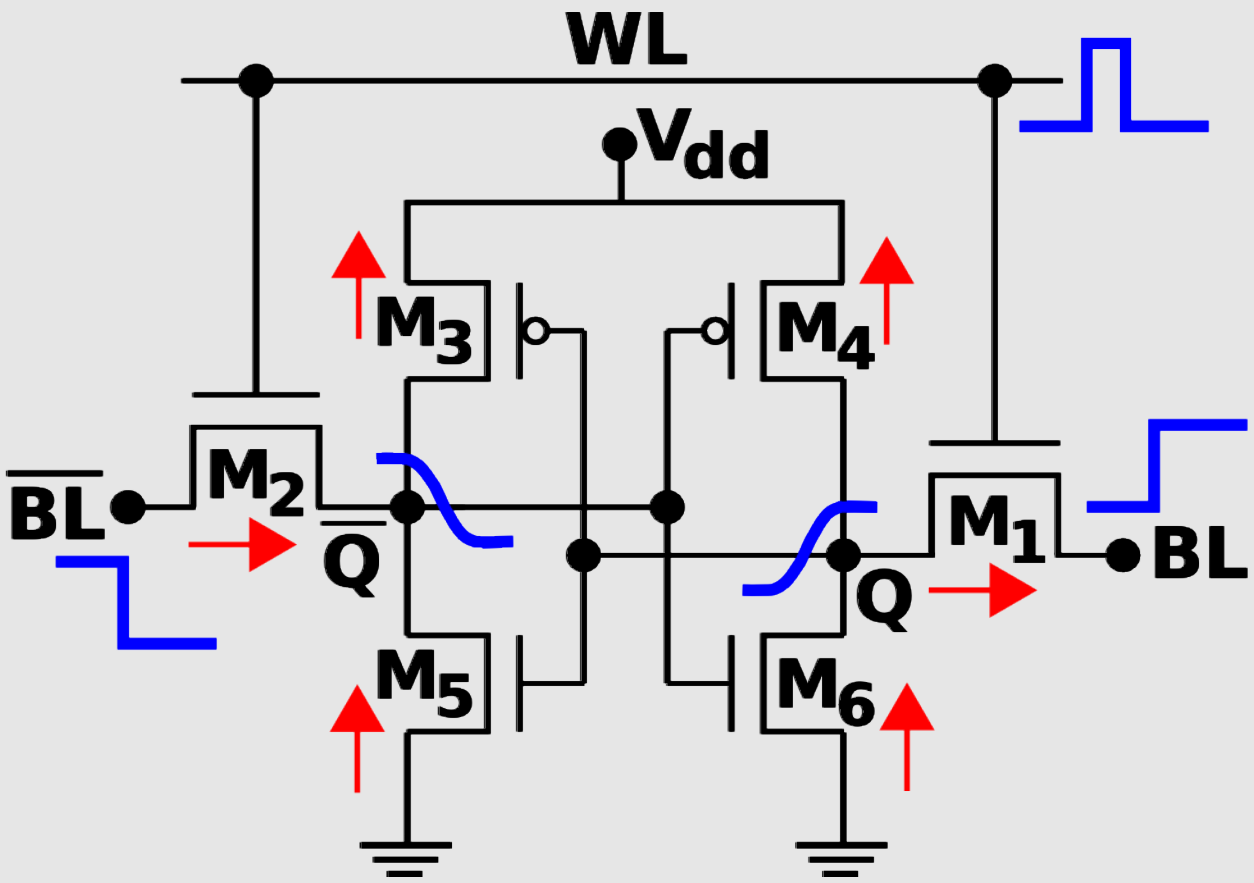
Billions of DRAM cells

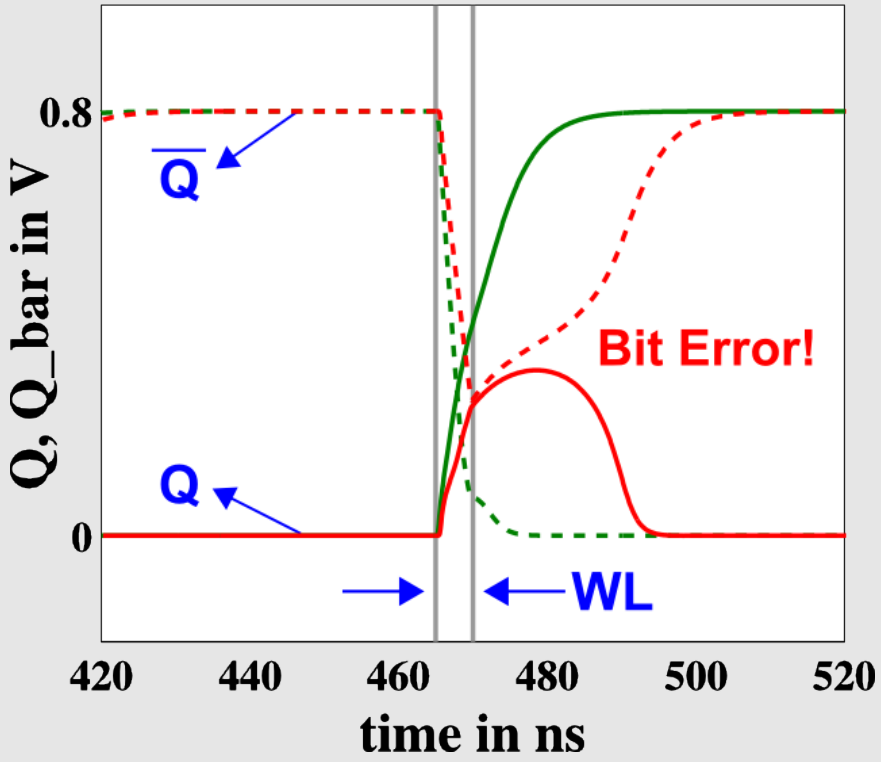
6T SRAM cell: Write Operation



- Key idea: Back-to-back inverters
- Writing a 1 to the SRAM cell
  - Switch BL to high, BL_bar to low
  - Briefly enable WL
- By the end of the clock cycle
  - Q should settle to 1
  - Q_bar should settle to 0
- Cross-coupled inverter pair will maintain this (stable) state

How RTN can impact SRAM write

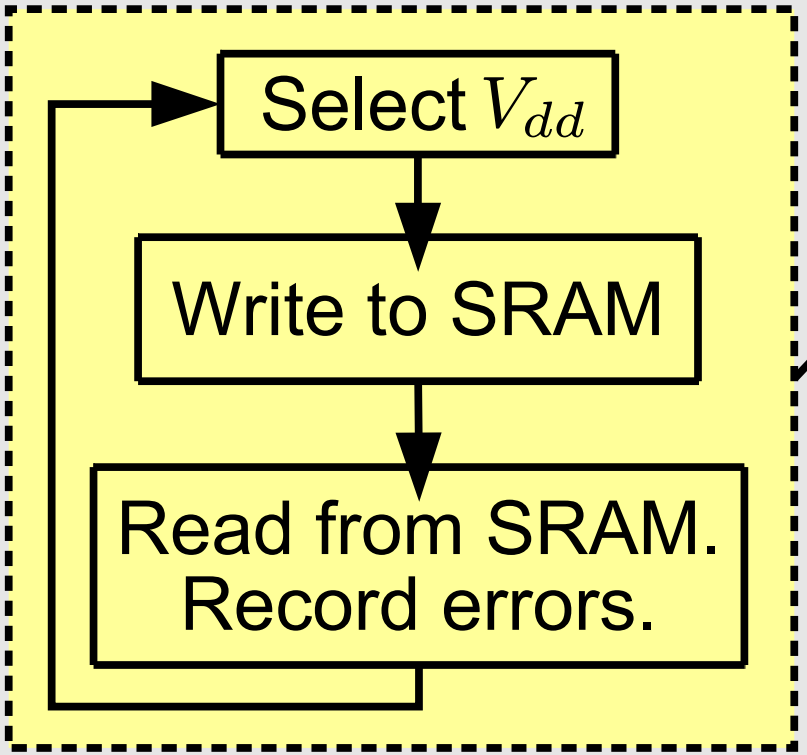




RTN can induce dynamic SRAM write failure!

(read failures also reported)

RTN in SRAMs: Experimental Evidence



For each V_{dd}, record min, max fail bit count

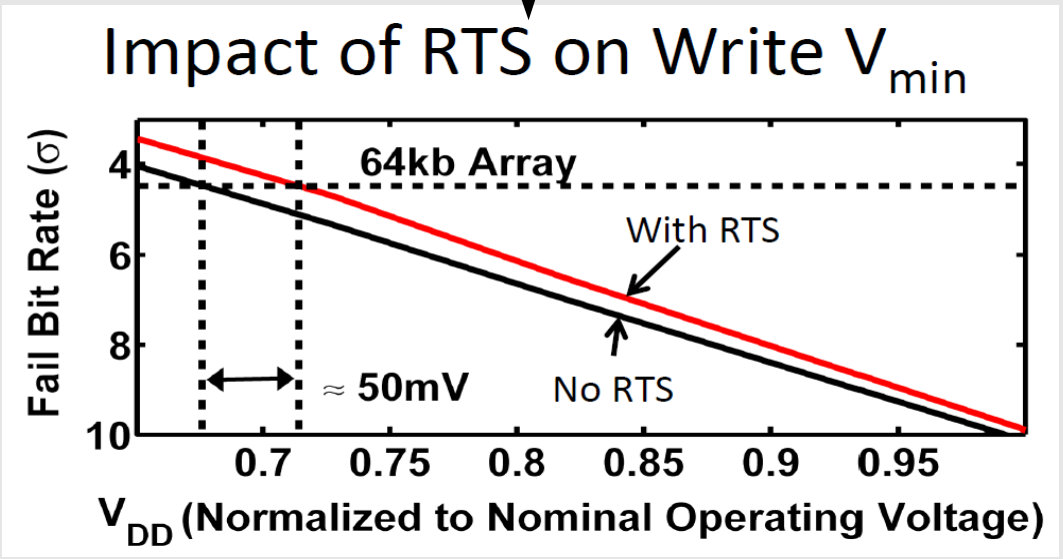
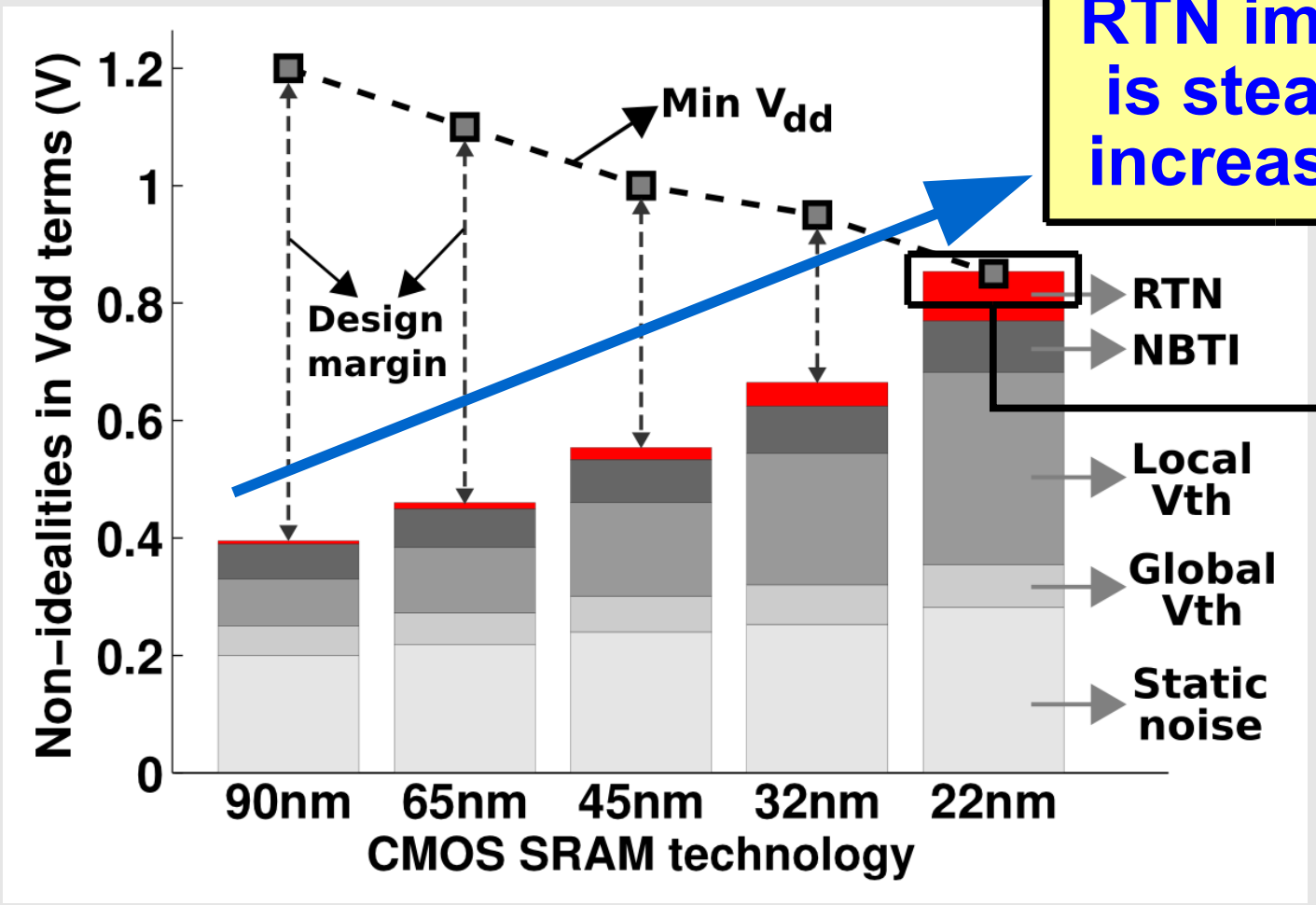


Fig. Credit: Seng O. Toh, PhD thesis, UCB

Measured data

- Confirms temporal SRAM failures due to RTN
- Quantifies RTN in V_{dd} terms at circuit level

Noise: An SRAM designer's viewpoint



RTN impact is steadily increasing!

$$\frac{1}{WL}$$

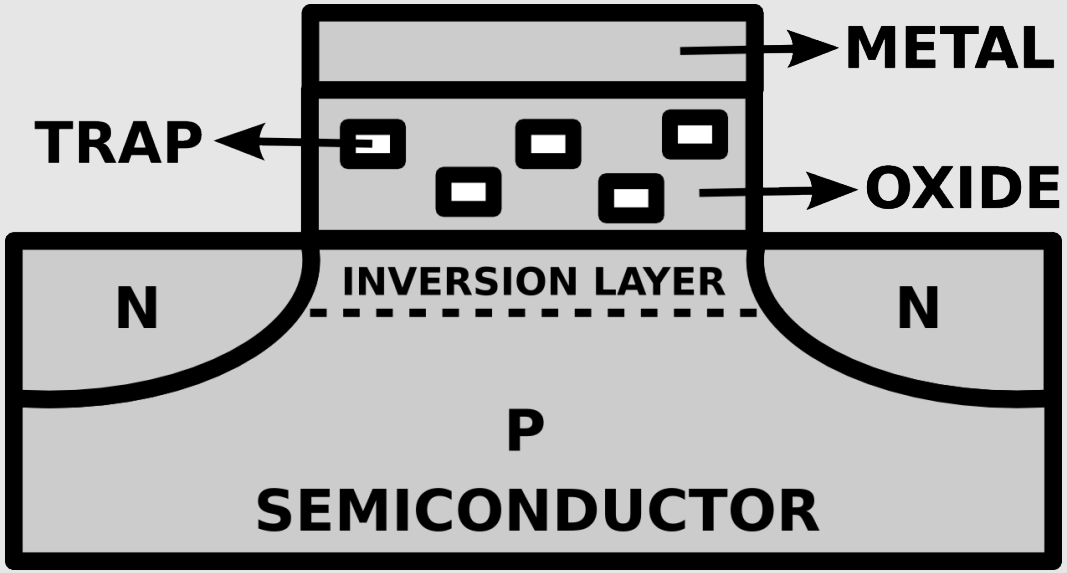
At 22nm, RTN can drive design margins negative!

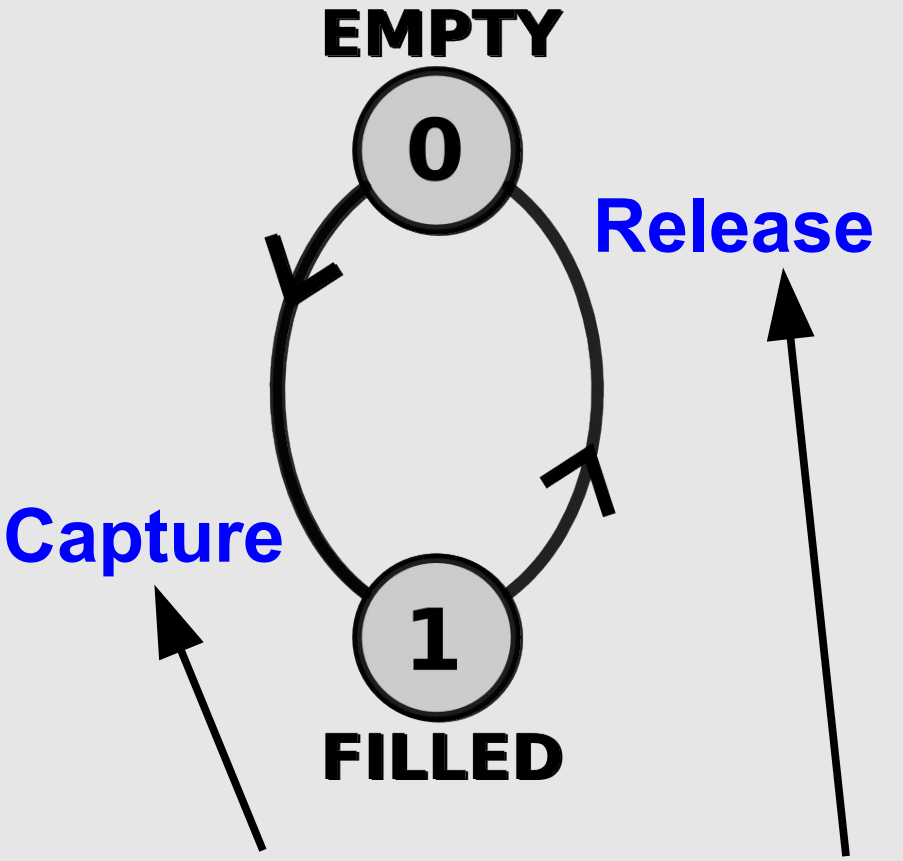
Figure credits: Y. Tsukamoto, Renesas Electronics Corp.

RTN-induced SRAM failures experimentally reported

Seng et. al. (IEDM 2009), Yas et. al. (IRPS 2010)

What causes RTN?

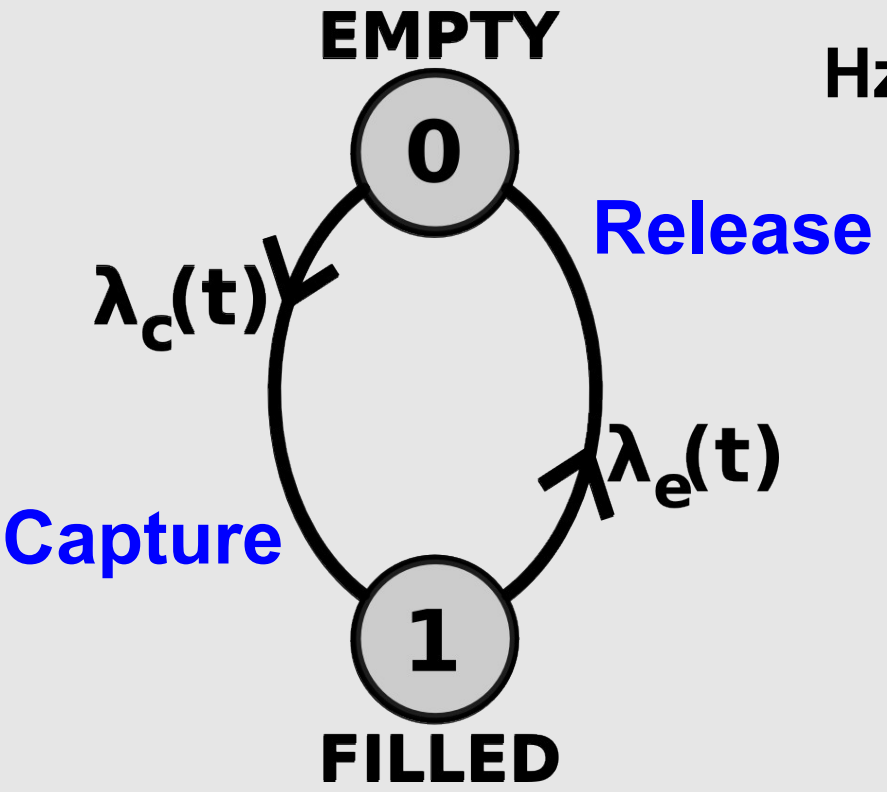


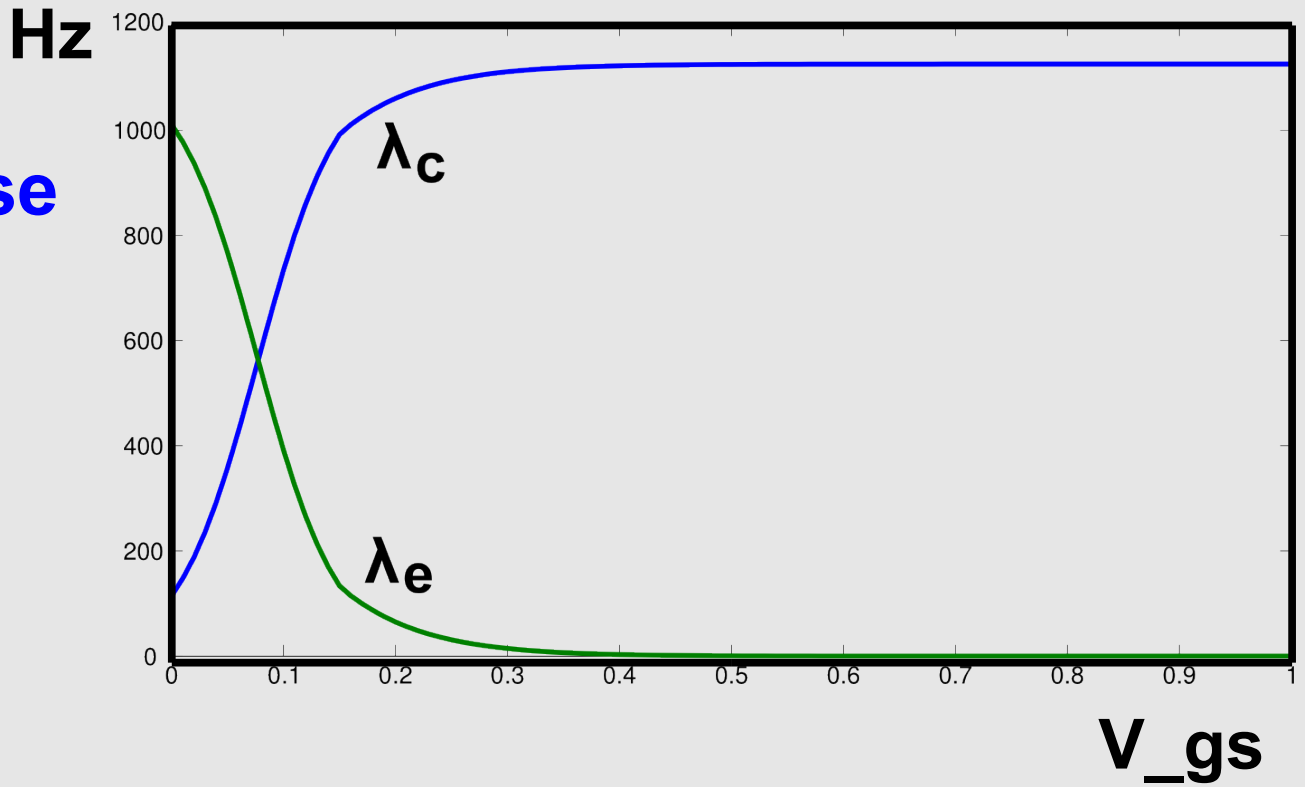


Filled traps modify number, mobility of electrons in inversion layer

Change in drain current → Measured as RTN

RTN is Non-Stationary





$$\lambda_c(t) + \lambda_e(t) = 1/(\tau_0 e^{\gamma y_{tr}})$$

$$\beta(t) = \lambda_e(t)/\lambda_c(t) = g\ e^{\frac{E_T - E_F}{kT}}$$

$$[(E_T - E_F)|_t = \text{function}(V_{gs}|_t)]$$

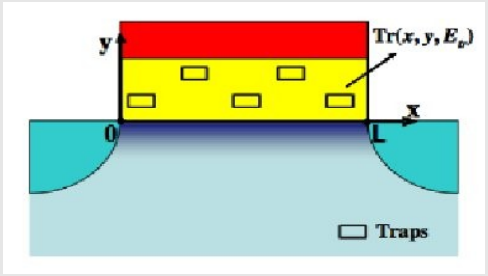
Bias-dependence leads to non-stationary RTN

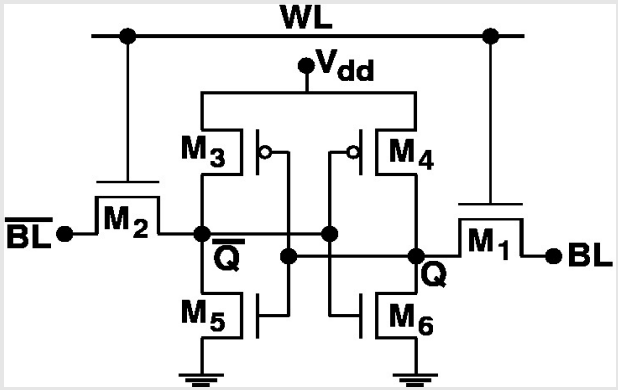
RTN: Bridging the Gap

Device level RTN models

MUSTARD

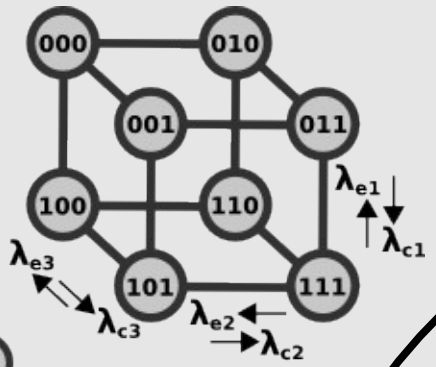
Circuit level RTN measurements

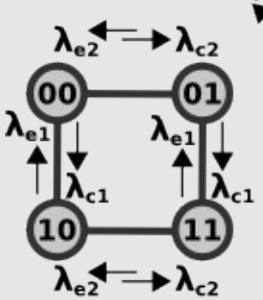




CAD tool incorporating device level RTN models for circuit level non-stationary RTN characterisation

MUSTARD's RTN Model





Markov state affects DAE's q(.), f(.)

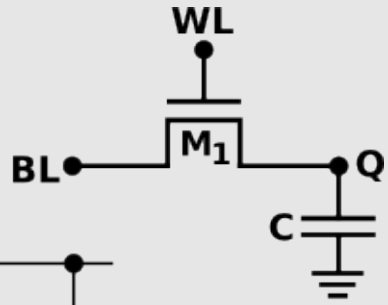
Continuous Deterministic

$$\frac{d}{dt}\vec{q}(\vec{x}) + \vec{f}(\vec{x}) + \vec{b}(t) = \vec{0}$$

Markov chain (RTN)

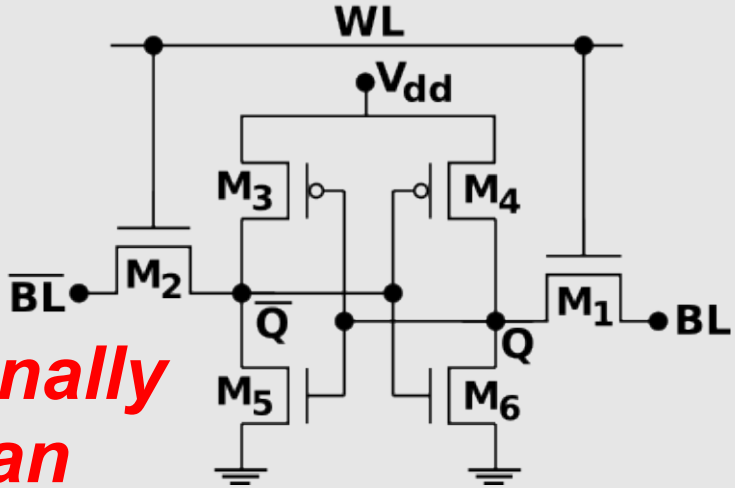
Coupled

Differential Algebraic Equations (Rest of the circuit)



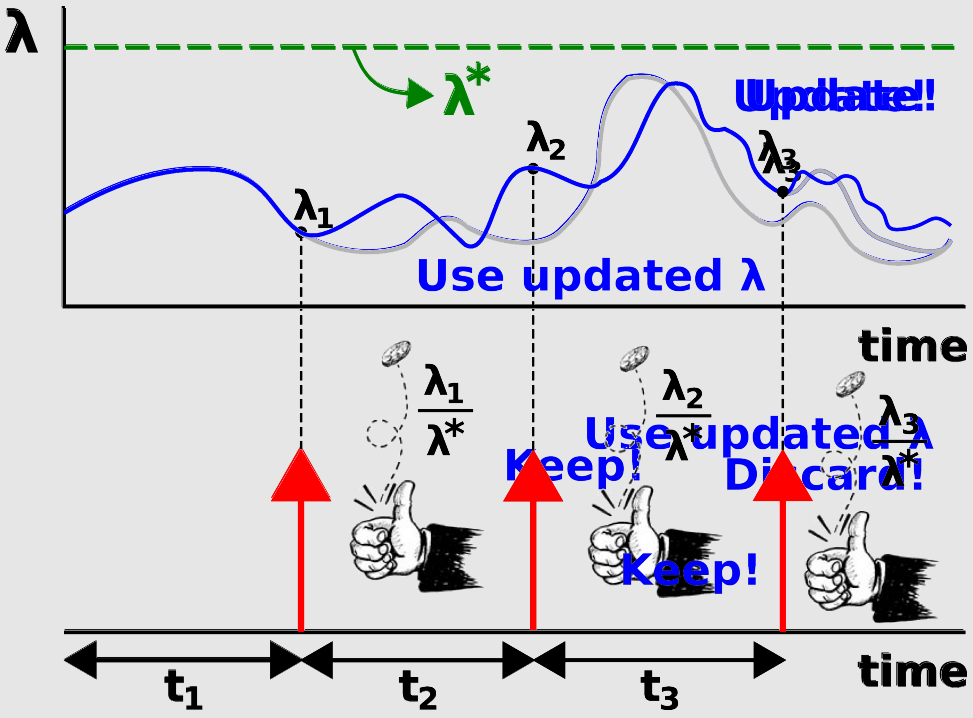
Discrete Stochastic

ongoing DAE solution affects Markov propensities



Core idea: Simulate the bi-directionally coupled MC-DAE system using an intelligent Monte-Carlo scheme

MUSTARD: Non-stationary Trap Simulation with Bi-Directional Coupling



Choose $\lambda^* \geq \lambda(t),\ \forall\ t$

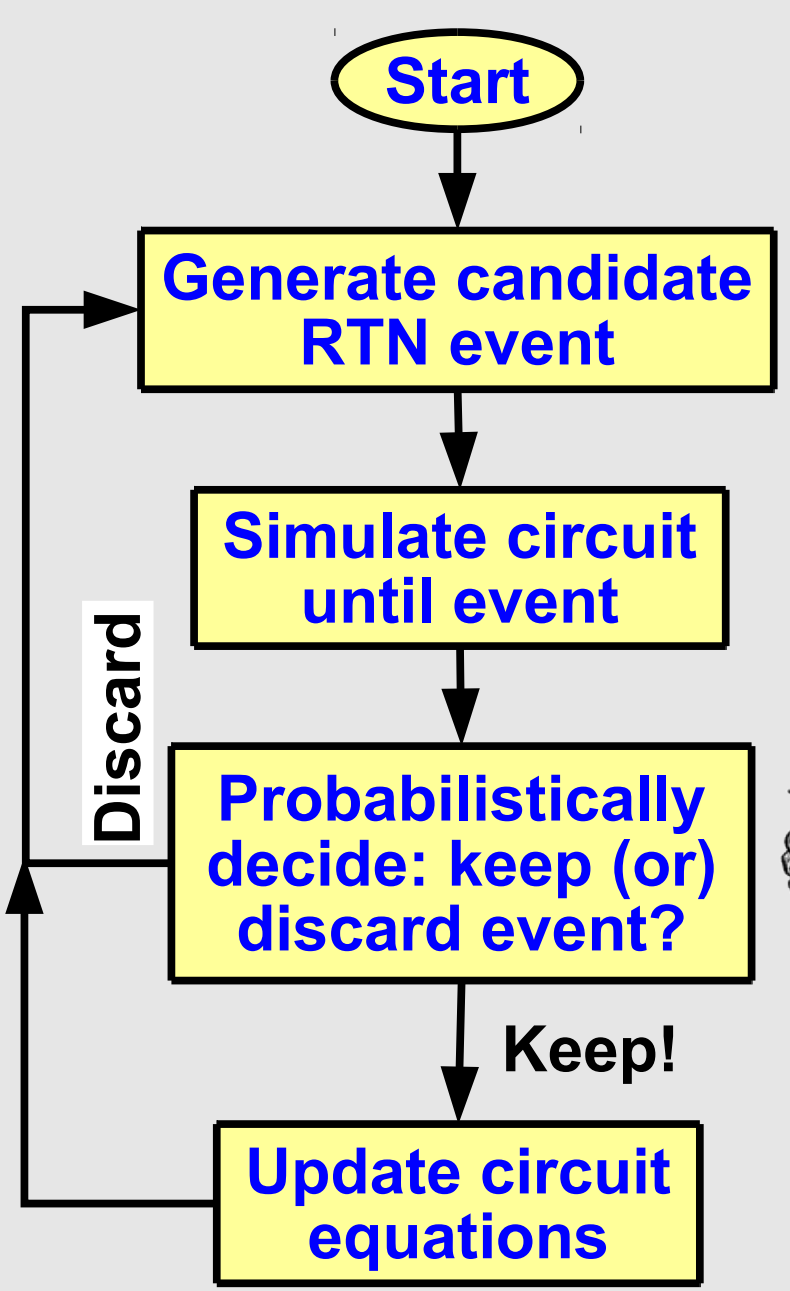
Generate exp. RV, mean $1/\lambda^*$
Find λ_1
Flip a coin, $\Pr(\text{heads}) = \lambda_1/\lambda^*$
Keep $\longrightarrow$ update rate

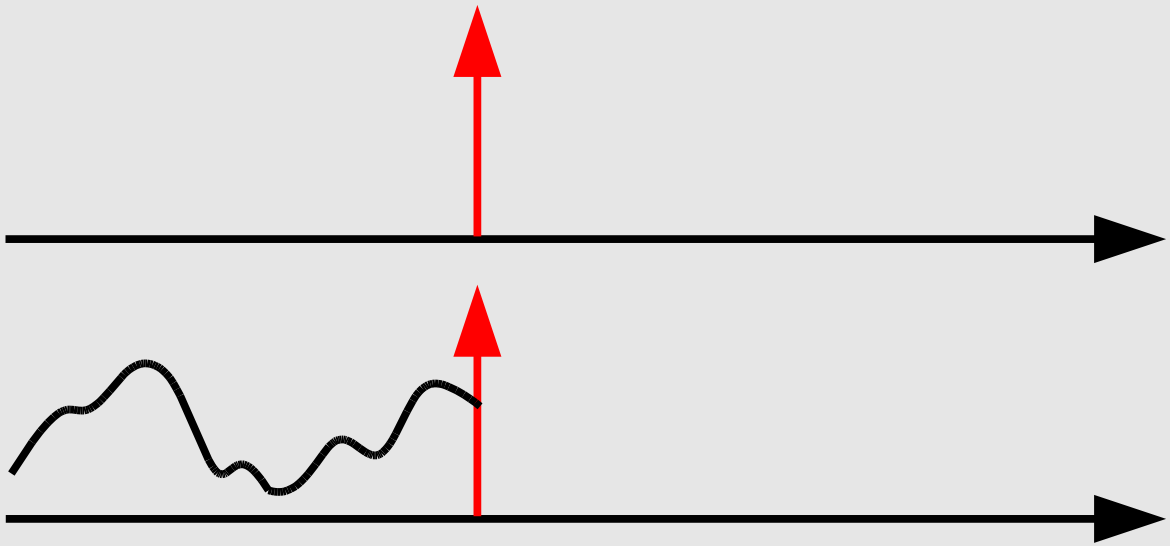
Generate exp. RV, mean $1/\lambda^*$
Find λ_2
Flip a coin, $\Pr(\text{heads}) = \lambda_2/\lambda^*$
Discard $\longrightarrow$ don't update rate

Generate exp. RV, mean $1/\lambda^*$
Find λ_3
Flip a coin, $\Pr(\text{heads}) = \lambda_3/\lambda^*$
Keep $\longrightarrow$ update rate

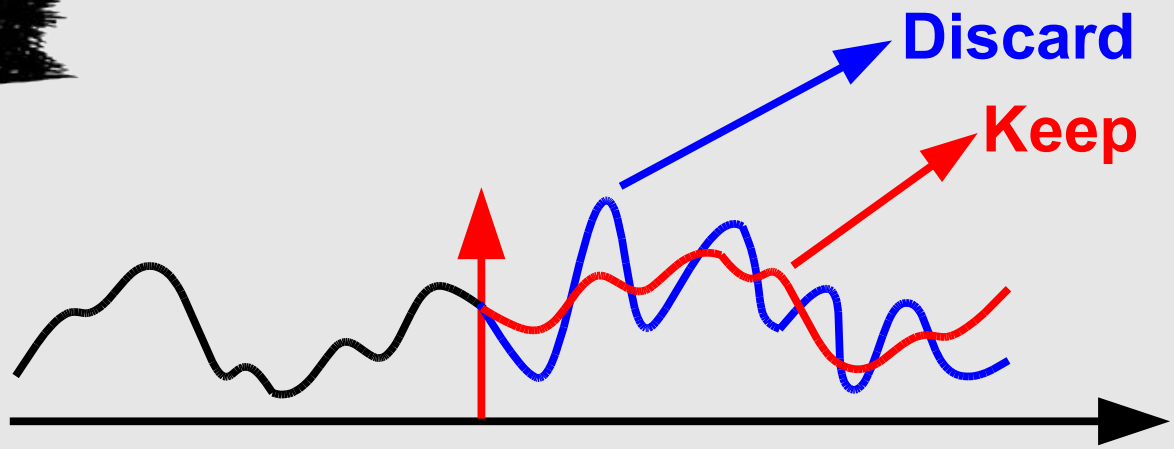
… and so on

MUSTARD: Simulation Methodology

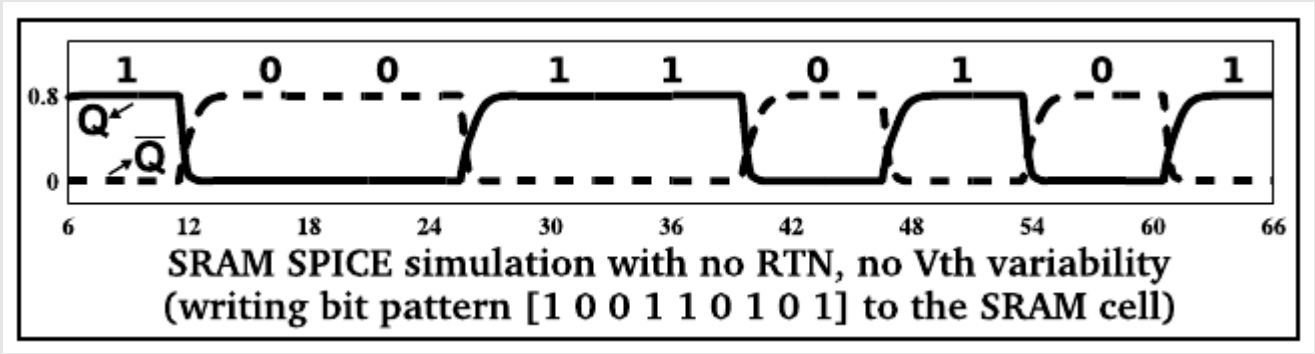




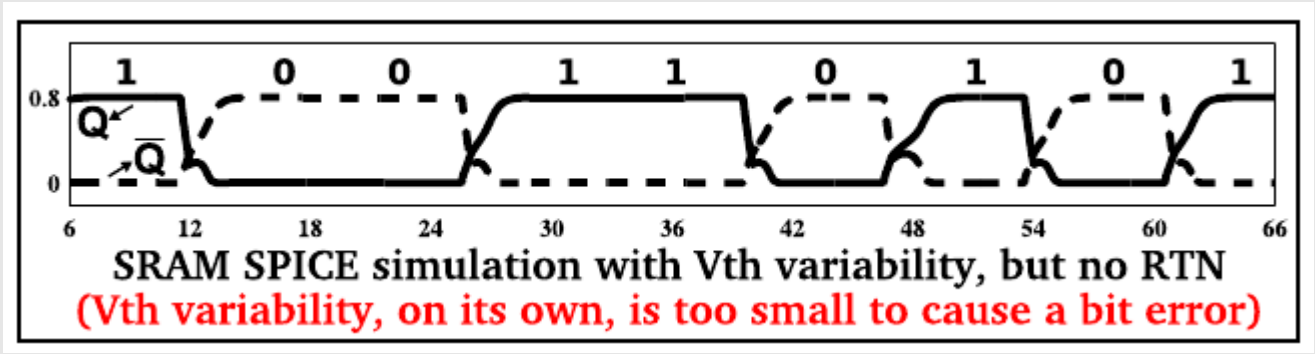
Exact, non-stationary statistics preserved!



MUSTARD: Individual SRAM cell



No RTN
No V_th variability



No RTN
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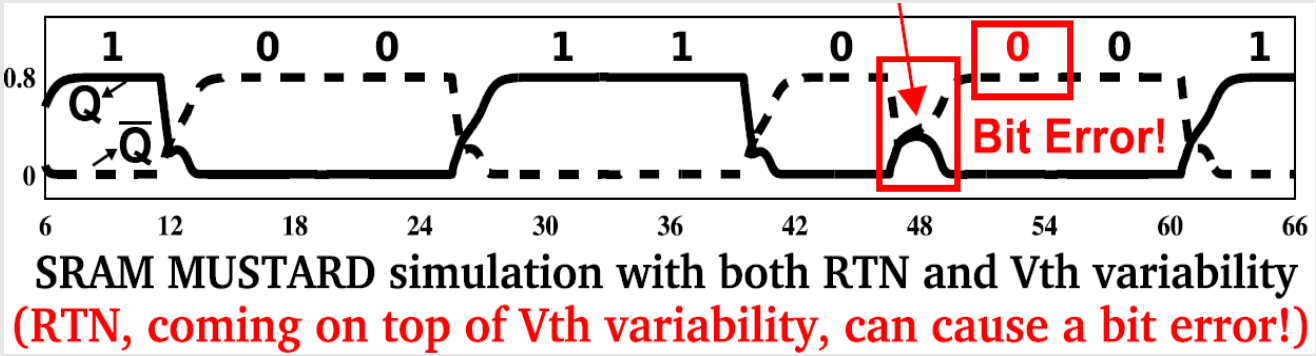
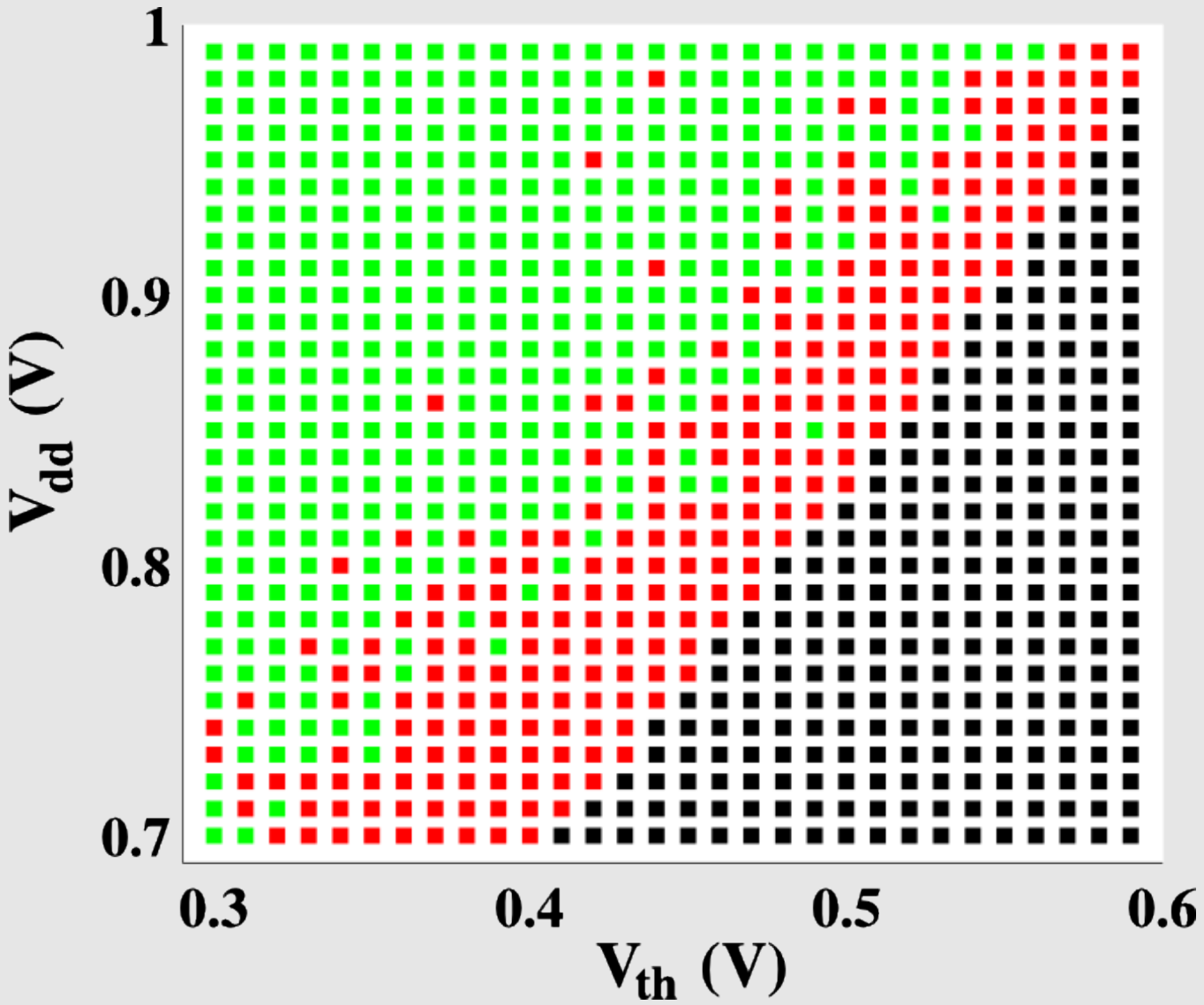


Yes RTN
Yes V_th variability

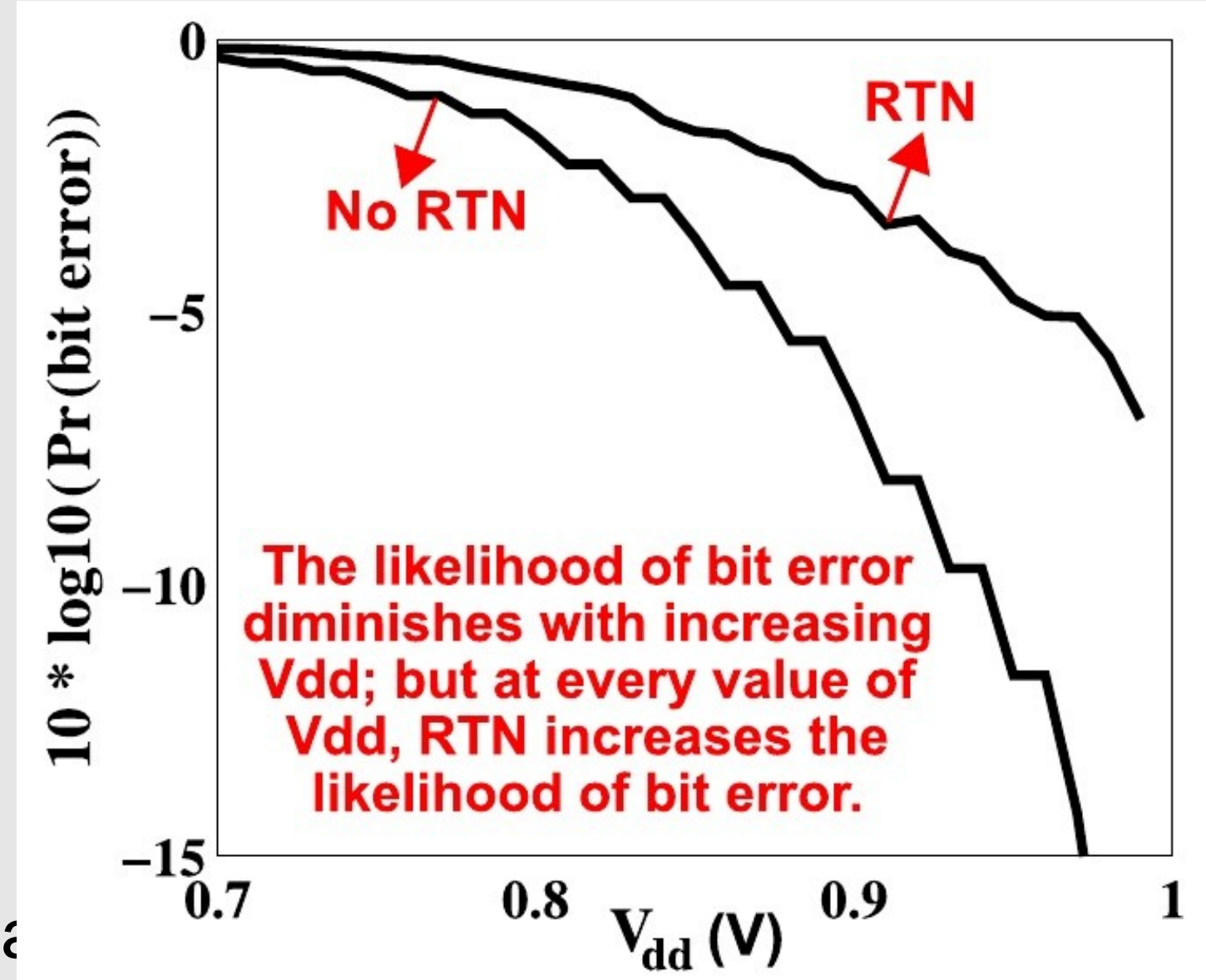
RTN+Variability: MUSTARD on 6T SRAM across (V_{DD},V_{th}) landscape



With RTN

Without RTN

MUSTARD-generated BER vs VDD plots



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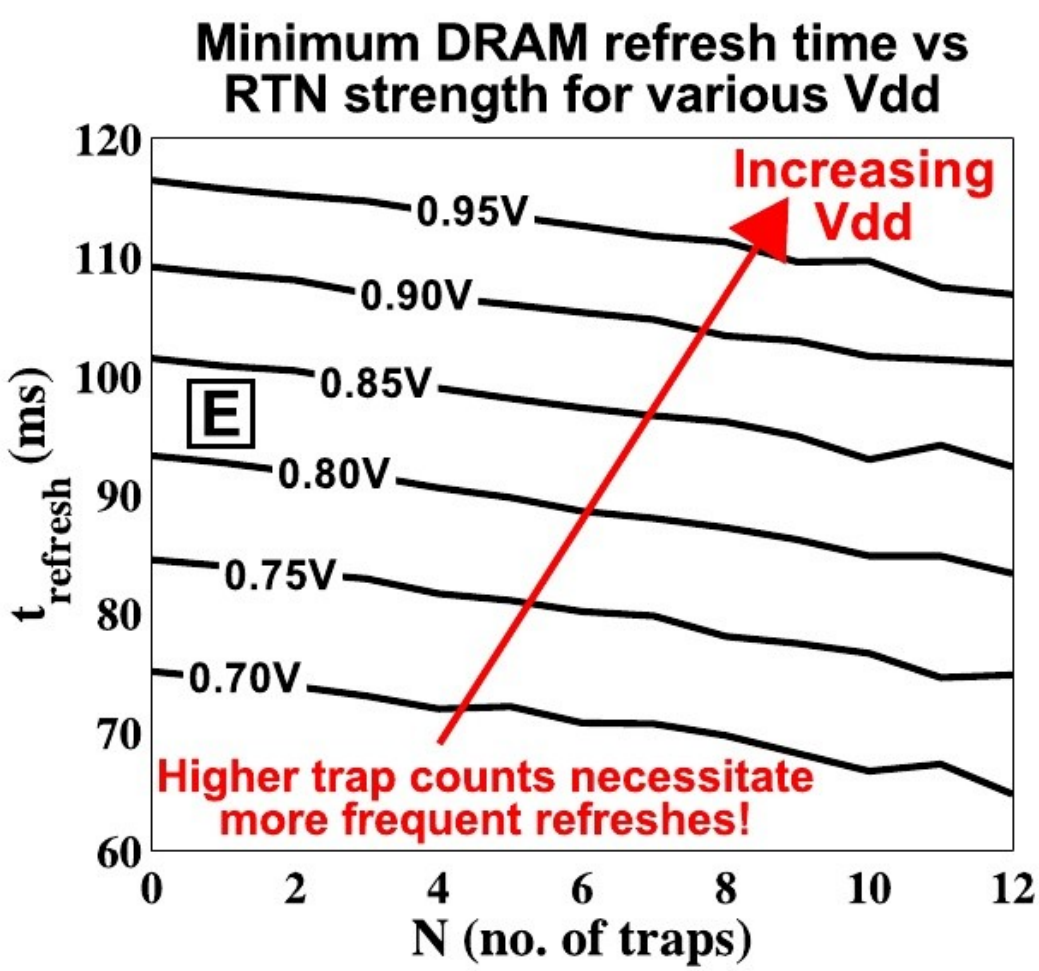
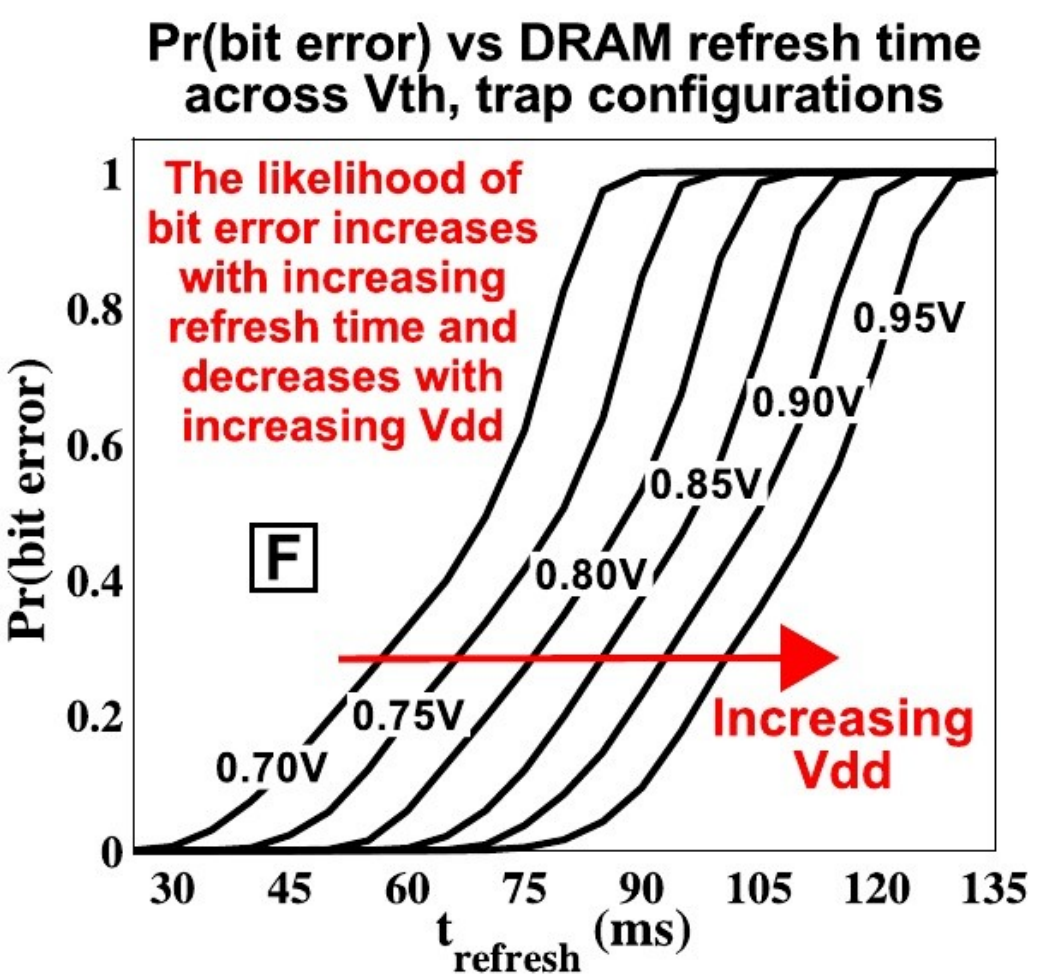
MUSTARD: RTN Effects on DRAMs





Summary and Conclusions

- RTN is a concern for SRAM scaling
- Bottom-up prediction of bit errors challenging
  - discrete random events + non-stationarity + “feedback”
- MUSTARD offers a simulation-based solution
  - strong mathematical guarantee on accuracy: applies to
    - any trap configuration
    - any circuit (SRAM, DRAM, etc.)
    - any device model, any model for RTN, etc.

Publications

(1) Aadithya V Karthik, Alper Demir, Sriramkumar Venugopalan and Jaijeet Roychowdhury. *SAMURAI: An accurate method for modelling and simulating non-stationary Random Telegraph Noise in SRAMs.* In Proceedings of the Design, Automation and Test Conference in Europe, 2011.

(2) Aadithya V Karthik, Sriramkumar Venugopalan, Alper Demir and Jaijeet Roychowdhury. *MUSTARD: A coupled, stochastic-deterministic, discrete-continuous technique for predicting the impact of Random Telegraph Noise on SRAMs and DRAMs.* In Proceedings of the Design Automation Conference 2011.

(3) Aadithya V Karthik, Alper Demir, Sriramkumar Venugopalan, and Jaijeet Roychowdhury. Accurate Prediction of Random Telegraph Noise Effects in SRAMs and DRAMs. In the 2013 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 32, Issue 1.