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Variation-aware Fault Modelling and Simulation for Deep-Submicron Manufacturing Defects

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Outline

- Effect of process variation
  - ✓ Manufacturing Test
- Research focus
- Methodology
- Results
- Conclusion

Effect of Process Variation

- Impact of fabrication process variation cannot be ignored
  - Circuit performance
  - Manufacturing test
- Manufacturing test
  - Increase in size of fault domain
    - ✓Fault simulation complexity increases
    - ✓Up to 10% loss of fault coverage using 1-detect test [TCAD 2009]
      - Traditional N-Detect test leads to large test size

Effect of Process Variation

Using SPICE on Intel Xeon Quad Core 2.7 GHz Processor with 12 GB RAM

Design	# of Gates	# of Bridge defects	Time (Days) using SPICE
C7552	762	581	15.34
S35932	3,734	1,194	32.04
S38584	5,251	2,965	77.4 (Estimated)

Design	# of Gates	# of Open defects	Time (Days) using SPICE
B10	100	113	1.77
B12	658	665	10.95
Usb_funct	5,142	5,745	93.36 (Estimated)

Cluster computing?

Effect of Process Variation

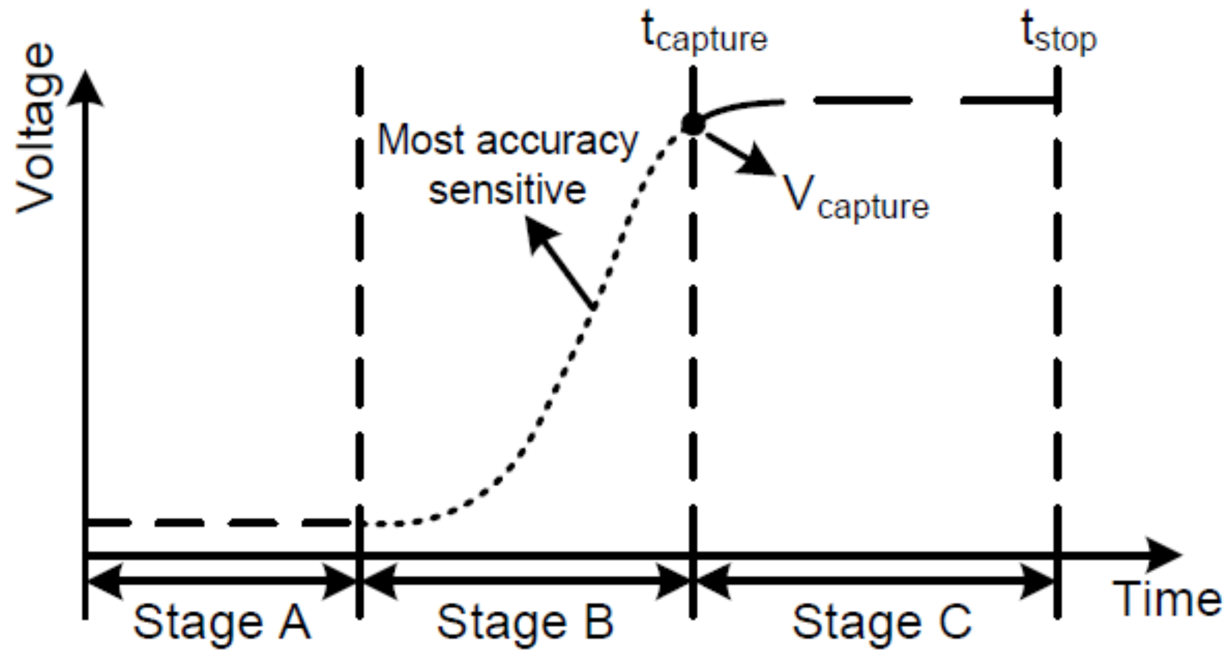
- Cluster computing
  1. About a week with 8-node cluster to compile fault information for ISCAS 85, 89 benchmarks. [Trans CAD, 2009]
  2. Ten days with a 32-node cluster to compile fault information for simple logic gates. [Springer Journal, 2011]

Can we do better?

How?

- Speedup is achieved by employing the following strategy:
  1. Identify key variables for computing delay fault
     - ✓Logic threshold voltage
     - ✓Transient gate output voltage
  2. Using NGSPICE (open source), only necessary transistor models and parameters are retained
     - ✓ BSIM 4.7 transistor model is used for accuracy
  3. Bisection algorithm to further reduce convergence time for computing delay faults

How?



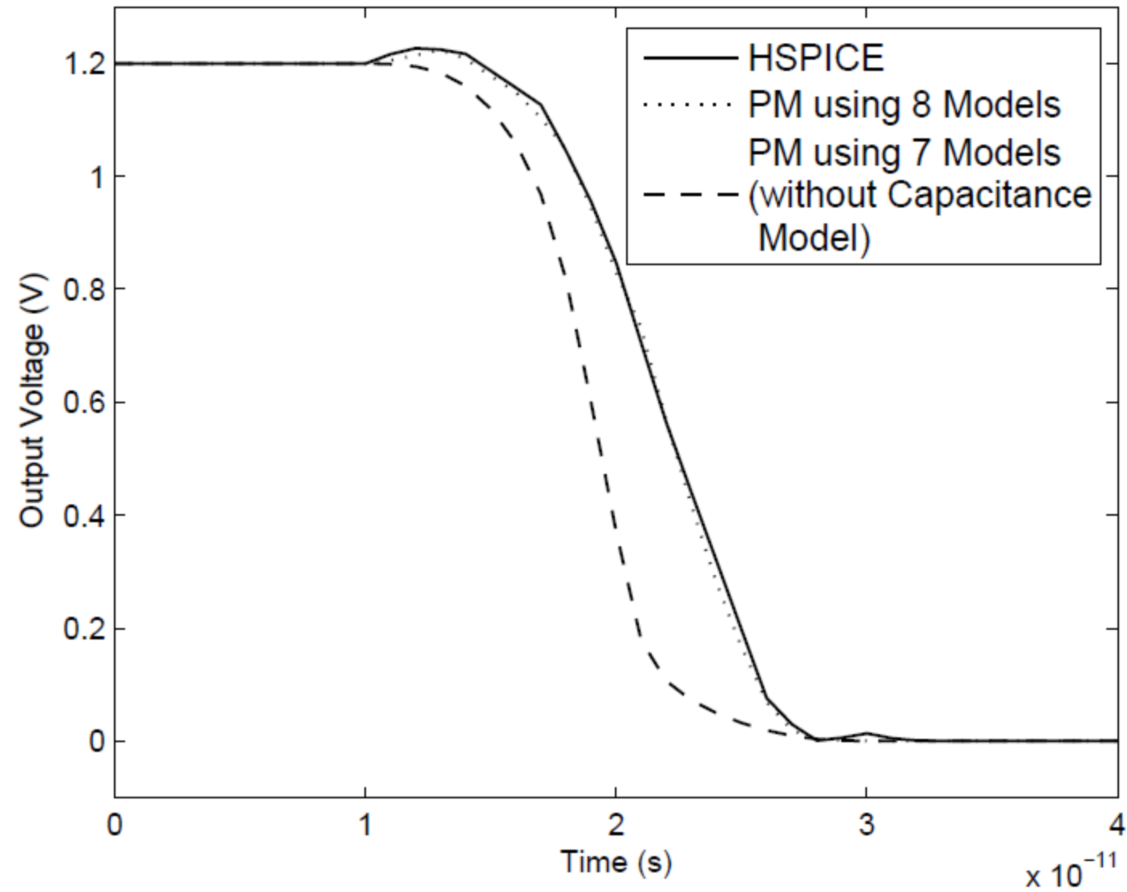
- "Stage B" is the most accuracy sensitive and time consuming stage

How? Step 1/3

Transistor Models in BSIM 4.7	Model Used	Parameter Used	Loss of Accuracy
Drain Current	√	92%	0.42%
Channel Charge & Subthreshold	√	75%	0.24%
Gate Direct Tunneling Current	√	90%	0.34%
Capacitance	√	80%	0.51%
Threshold Voltage	√	100%	0%
Body Current	√	100%	0%
Temperature Dep	√	100%	0%
Layout-Dependent Parasitics	√	100%	0%
Asymmetric Junction Diode	X		0.27%
New Material	X		0.03%
Stress Effect	X		0.08%
Well Proximity Effect	X		0.11%
High-Speed RF	X		0.03%
Noise	X		0.04%

- Transistor models and electrical parameters elimination

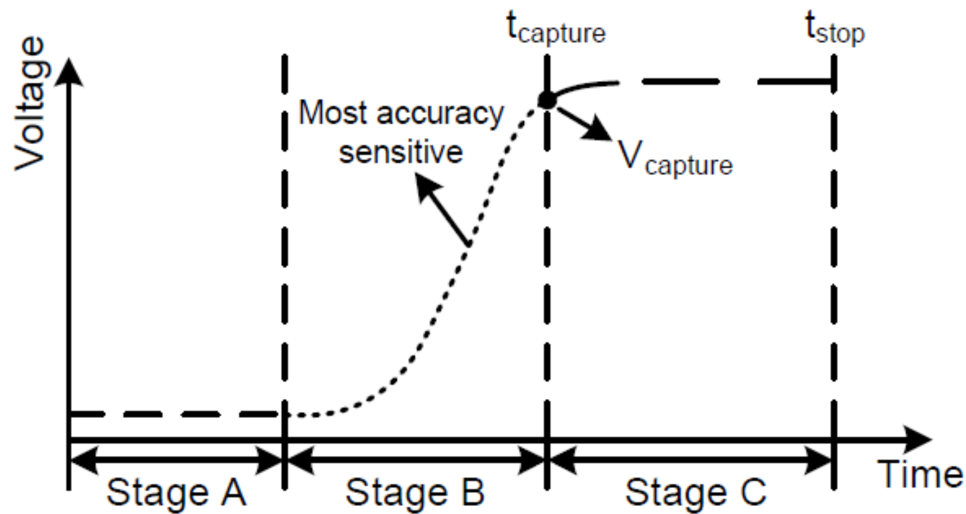
Effect on accuracy

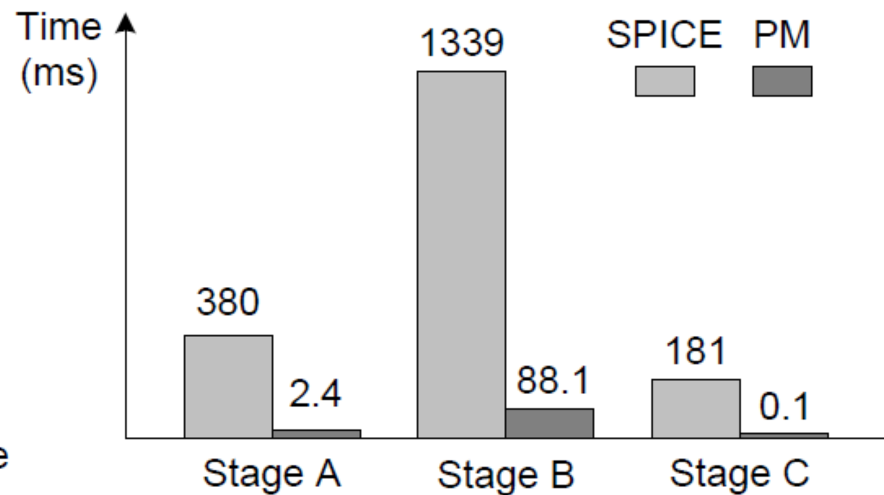


Effect of Transistor Model and Electrical Parameter Elimination

How? Step 2/3

- Step size adjustment



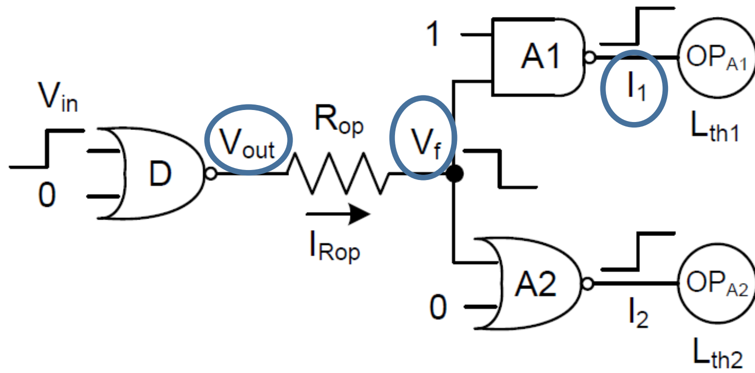


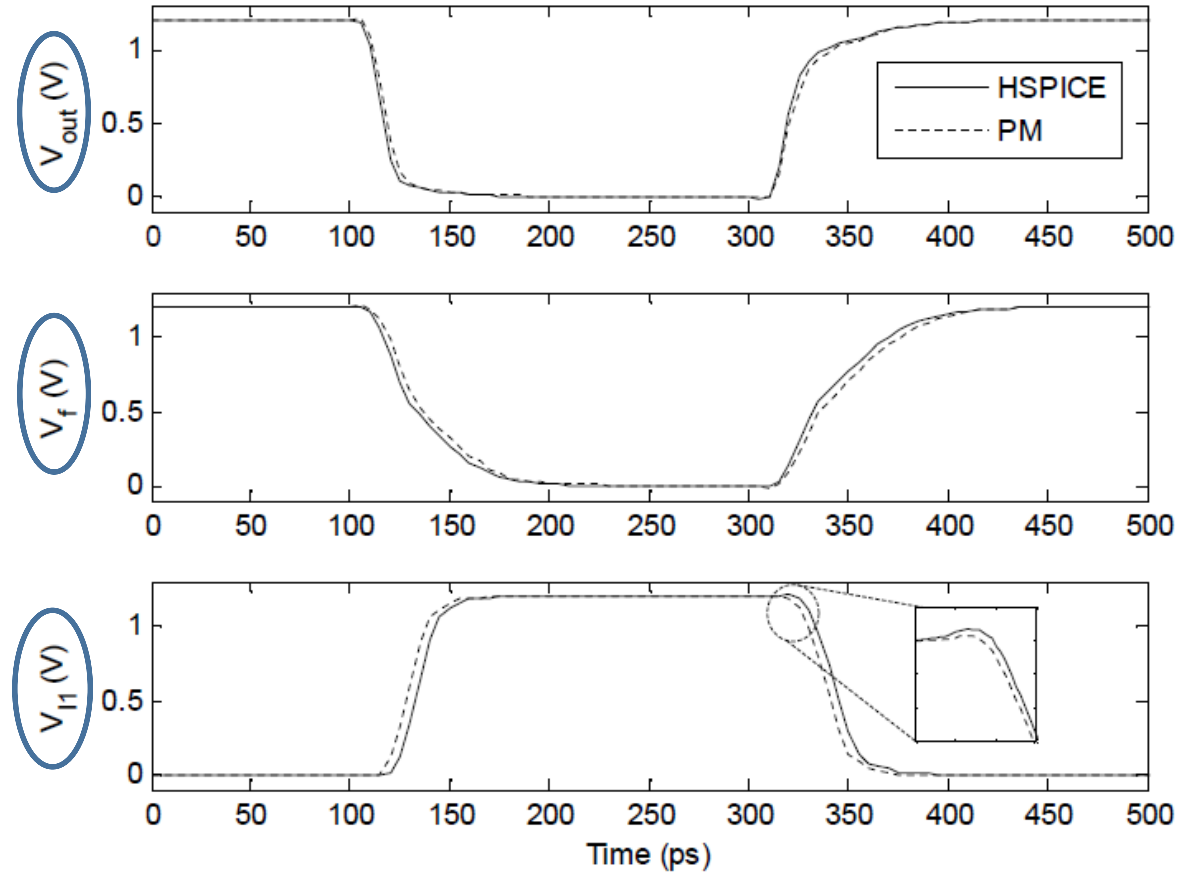
Relative Speedup in each of the three transient signal stages

Accuracy vs. Speedup

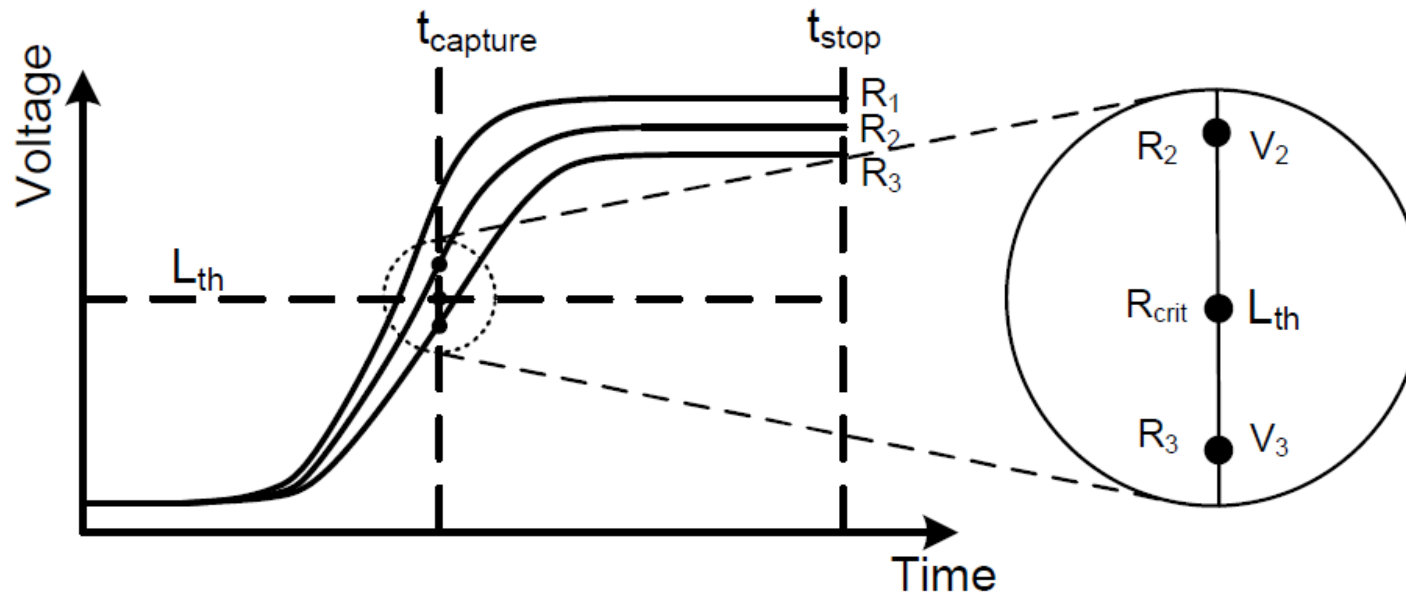
	Error (%)	Speedup
Models elimination	0.8	2.36
Parameters elimination (Step-1)	2.0	4.47
Step size adjustment (Step-2)	2.2	4.13
Combined effect	4.2	19.3

Effect on accuracy



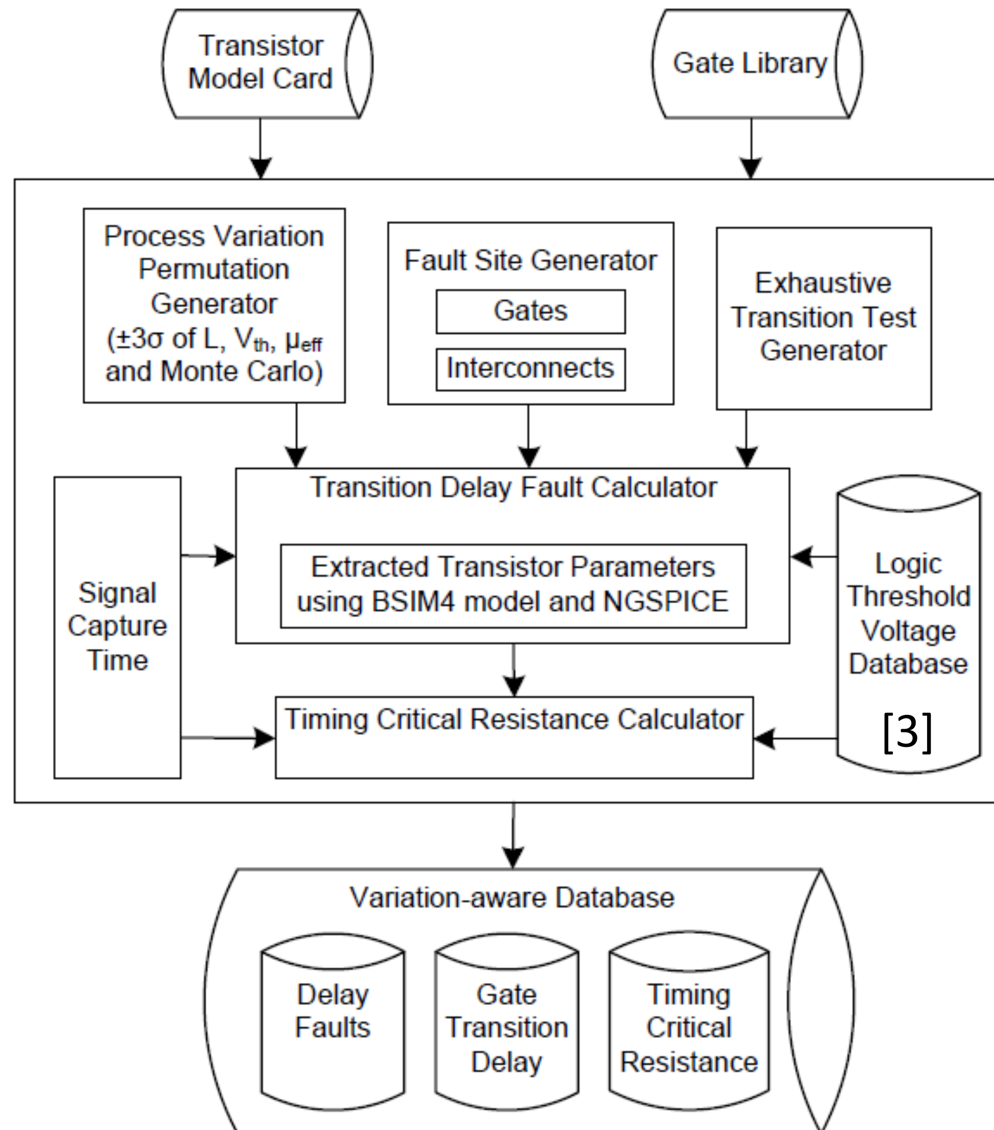


How? Step 3/3

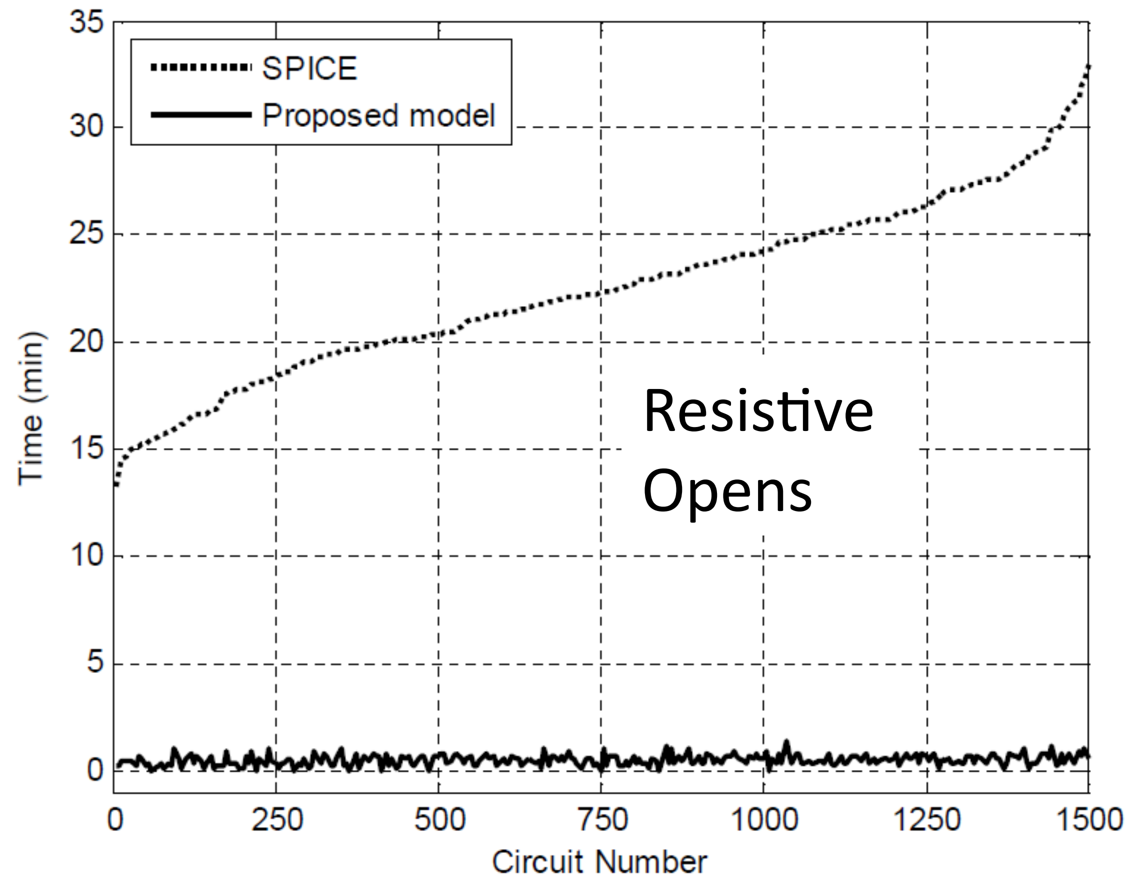


- An algorithm based on Bisection method is employed to compute timing critical resistance.

Simulation Flow



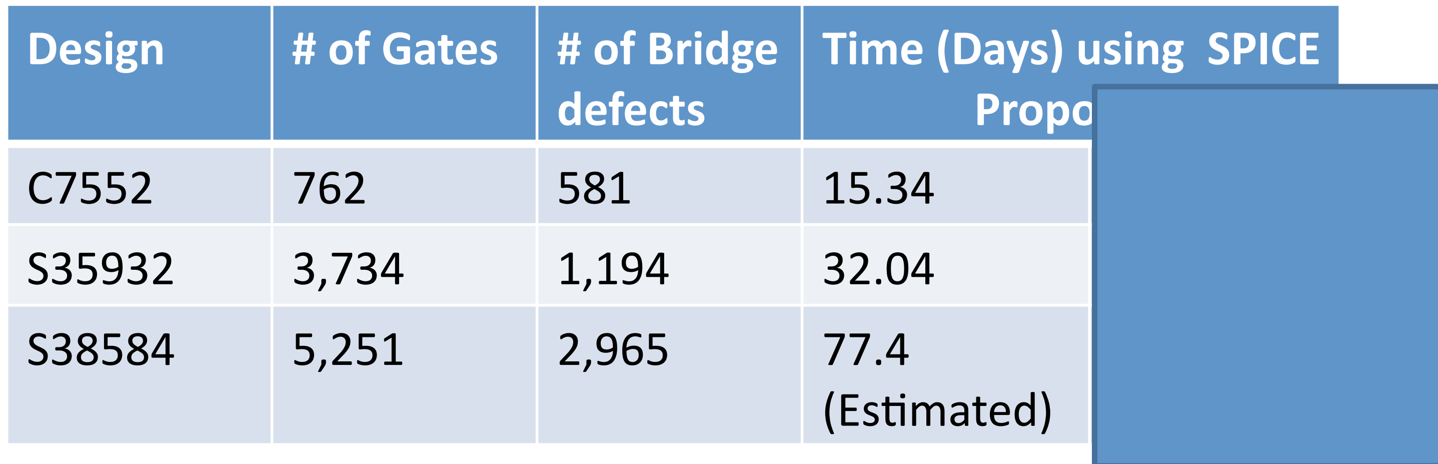
Results



Fault simulation method is on average 52-times faster than SPICE with ≤ 4% error in accuracy.

Results

Using Intel Xeon Quad Core 2.7 GHz Processor with 12 GB RAM



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Results using 60-node cluster

Design	# of Gates	# of Open defects	Time (Hours)
B19	52,005	56,672	8.41
Leon2	188,062	200,421	28.22
Leon3-avnet-3s1500	213,689	235,486	32.43

Conclusions

- Process Variation Aware Test
  a) Available fault simulation methods are time consuming, when considering the effect of Process, Voltage and Temperature (PVT) variations.
  b) New fault simulation methods have been developed for two most important deep submicron defects:
     - **Open Defects:** 52-times faster than SPICE with ≤ 4% error in accuracy.
     - **Bridge Defects:** 39-times faster than SPICE with ≤ 5% error in accuracy
  c) Useful for fault simulation (Histogram databases [2]), test generation and diagnosis of deep submicron defects under PVT variations.

Other activities …

1. Design for Test (DFT) architecture for power-gated designs to reduce test time and improve diagnosis accuracy.

2. Online test methods for improving fault tolerance capability of TSV based 3D ICs.

3. Reliability challenges for low power high performance designs
   - Caused by PVT variations and Soft Errors.

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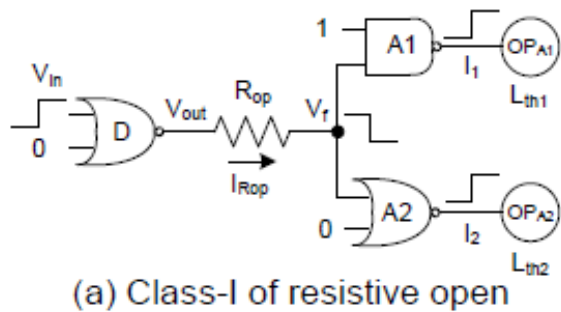
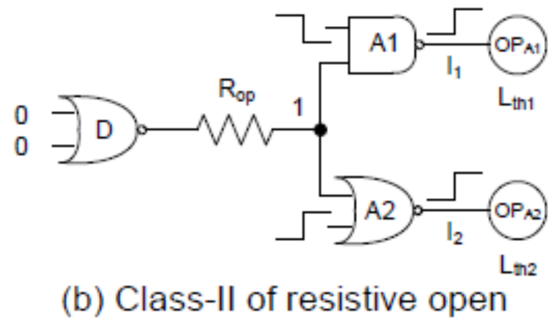
Thank you



(a) Class-I of resistive open



(b) Class-II of resistive open

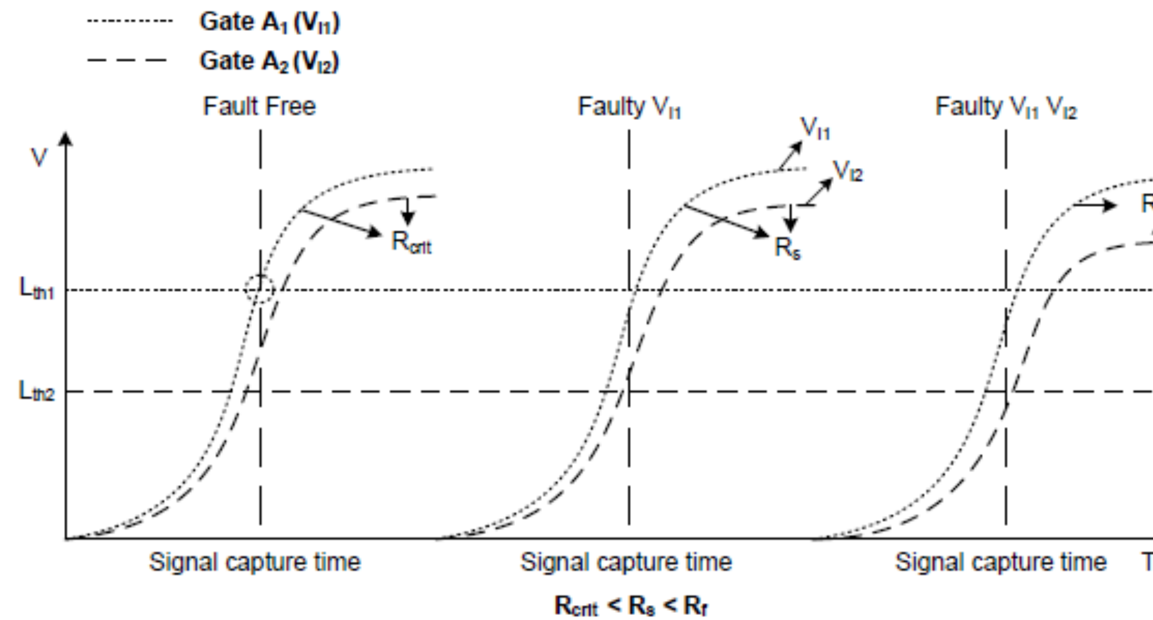


Fig. 2. Delay behavior of resistive open R_{op} in nominal operating conditi

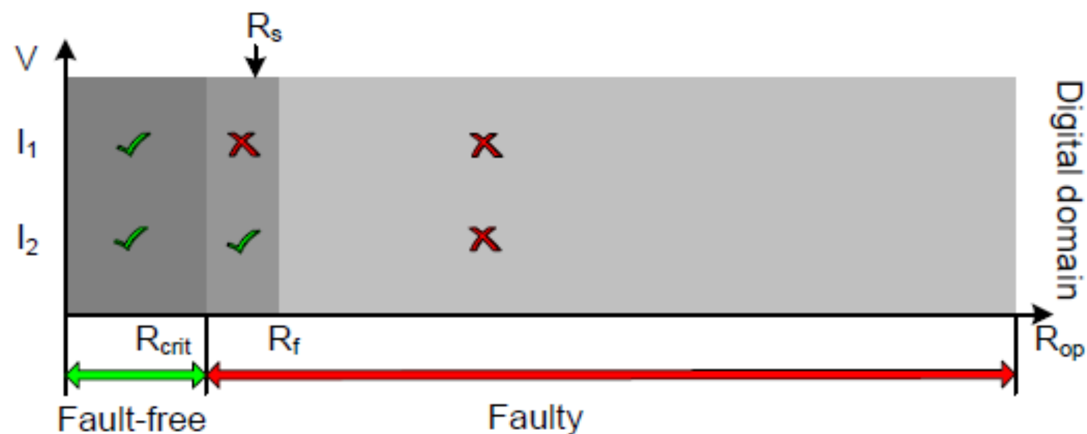


Fig. 3. Delay faults showing timing critical resistance determined through

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