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DOME

PAM: A Processor Ageing Model Based on Critical Path Delays

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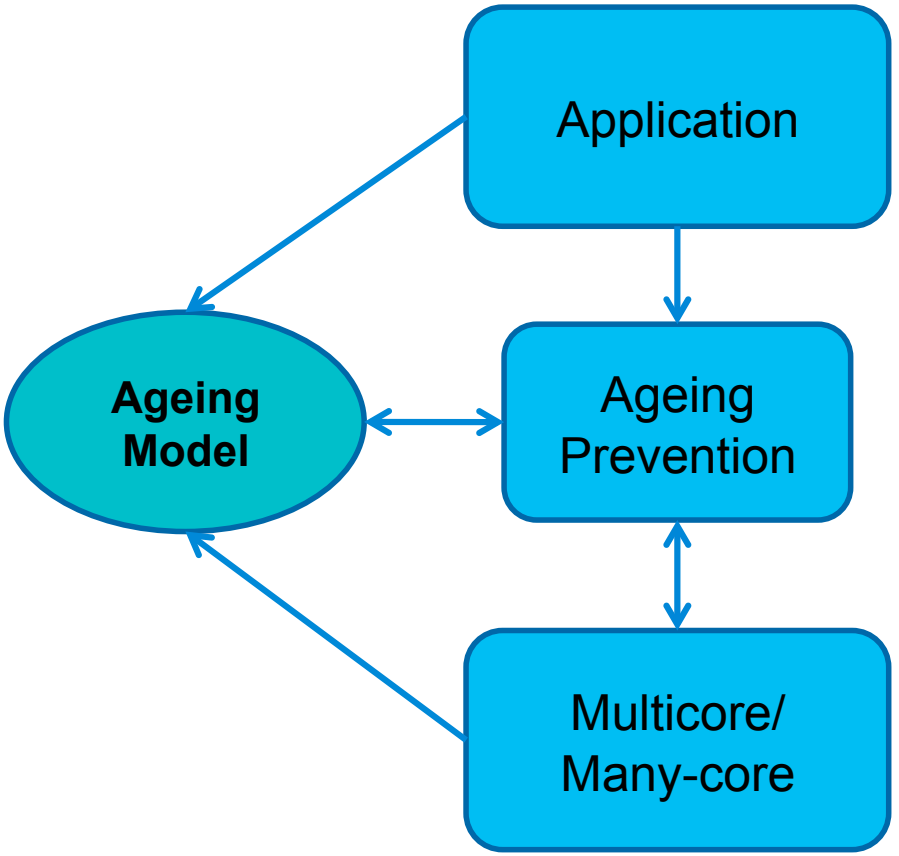
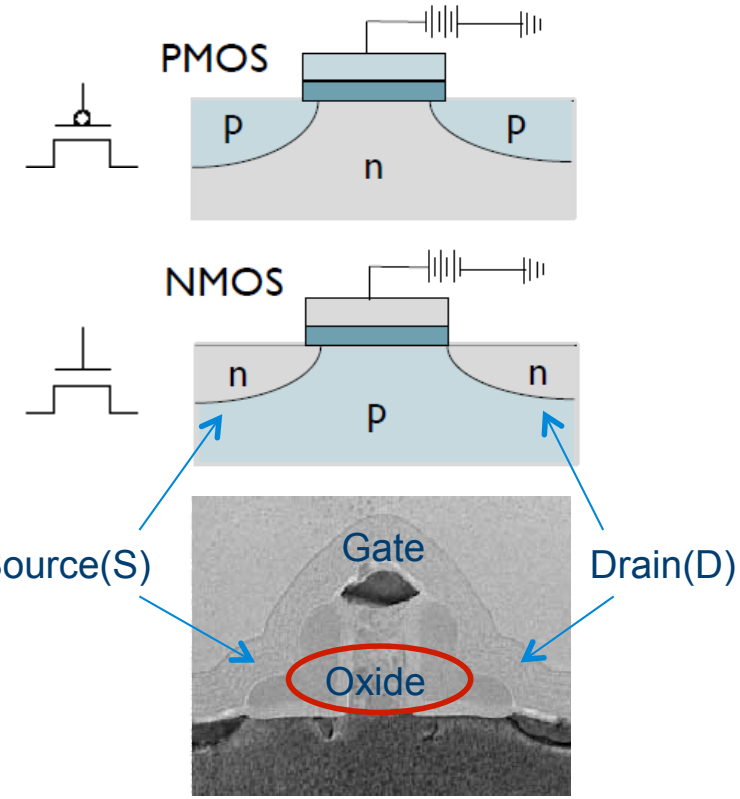
Agenda

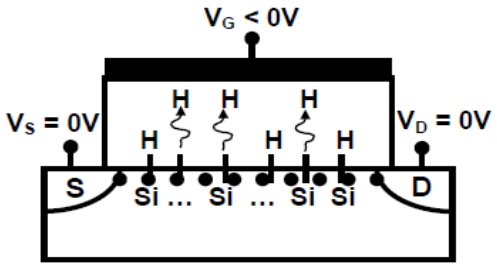
- Ageing model to characterise the applications' behaviour
- Micro-Architectural model
- Runtime based ageing prevention schemes



Transistor Ageing

- Major Failure Mechanisms



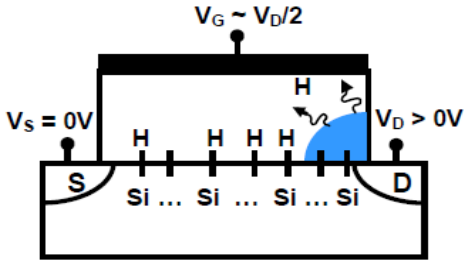


NBTI(PMOS)

Cold holes

Traps uniform in channel

SiH bonds



HCI (NMOS)

Hot carriers

Localized damage

SiH and SiO bonds

V_{th}

Transistor Ageing

- Ageing metric = Transistor switching delay

$$T_s \propto \frac{V_{dd} L_{eff}}{\mu (V_{dd} - V_t)^{\alpha}}$$

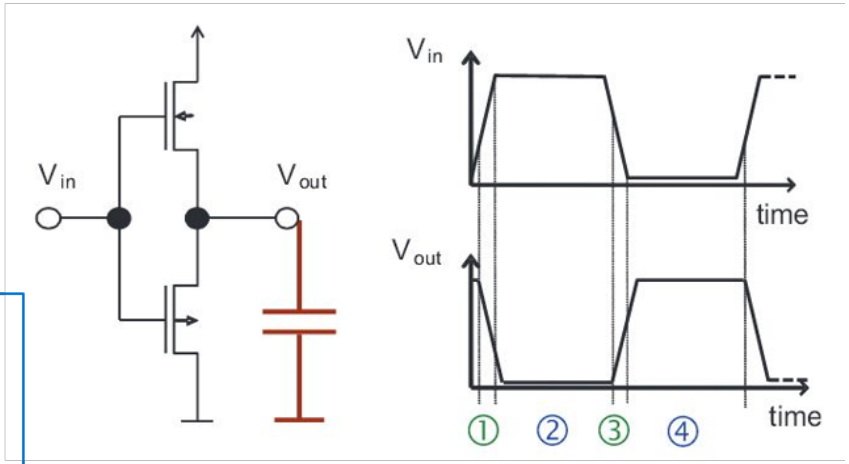
$$V_t = V_{th_0} + \Delta V_{th}$$

$$\Delta V_{th_{NBTI}} = \Delta V_{t_{stress}} \times \left(1 - \sqrt{\eta \times \frac{t_{rec}}{t_{stress} + t_{rec}}}\right)$$

$$\Delta V_{stress} = A_{NBTI} \times t_{ox} \times \sqrt{C_{ox}(V_{dd} - V_t)} \times e^{\frac{V_{dd} - V_t}{t_{ox} E_{ox}} - \frac{E_a}{kT}} \times t_{stress}^{0.25}$$

$$\Delta V_{th_{HCI}} = A_{HCI} \times \alpha \times f^{0.5} \times e^{\frac{V_{dd} - V_t}{t_{ox} E_1}} \times t_{act}^{0.5}$$

- The effect of NBTI and HCI in different regions of a CMOS inverter

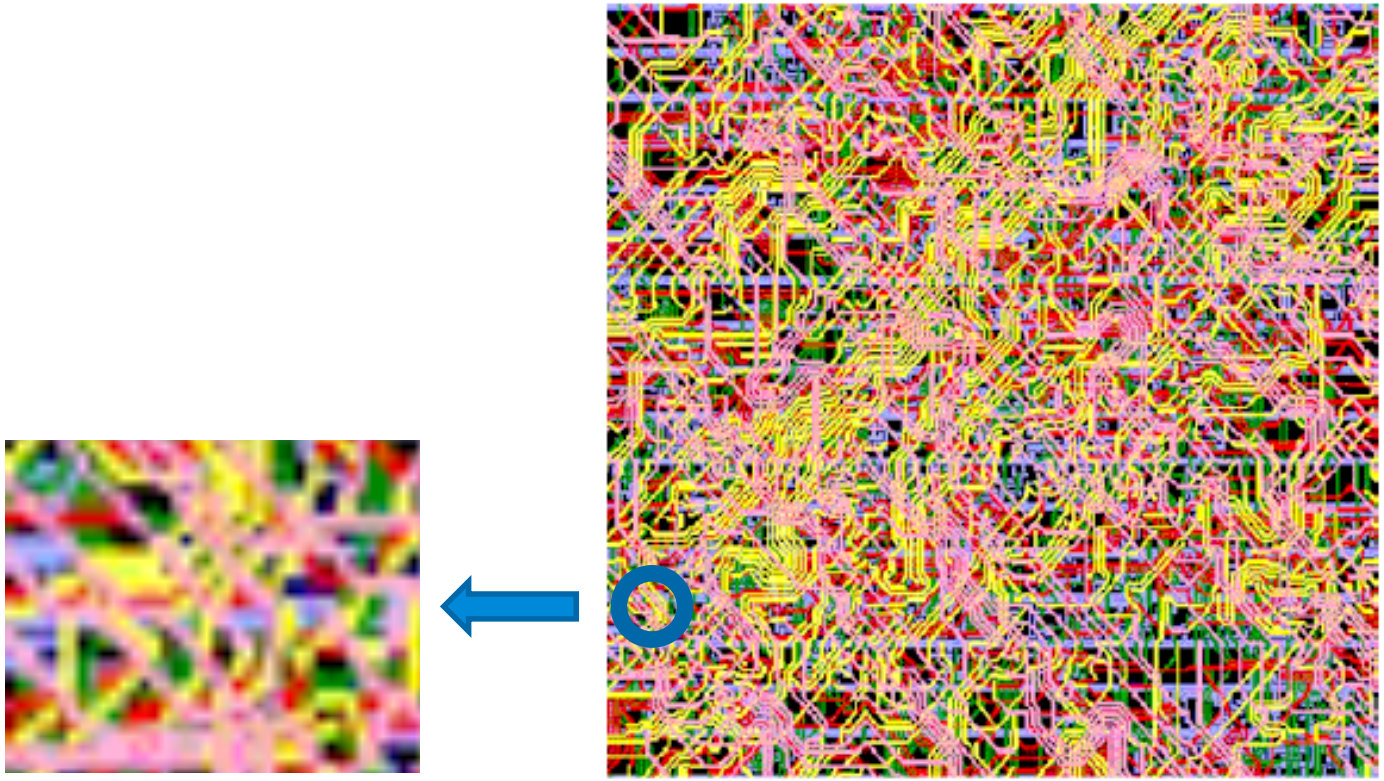


The Gaps in Knowledge

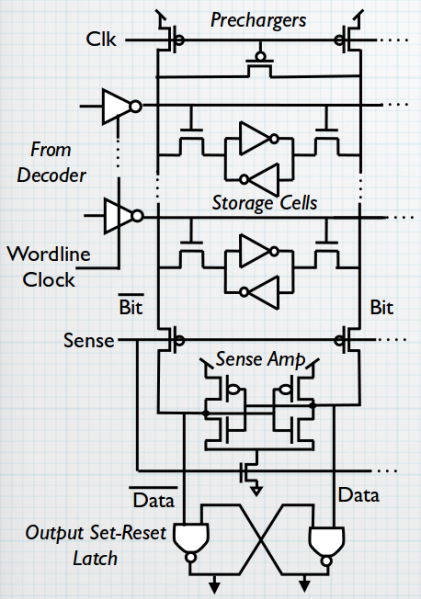
- Single core vs multicore and many-core
- Memory and cache vs processor
- All the units within the processor
- The level of implementation

Critical Path Delay Estimation

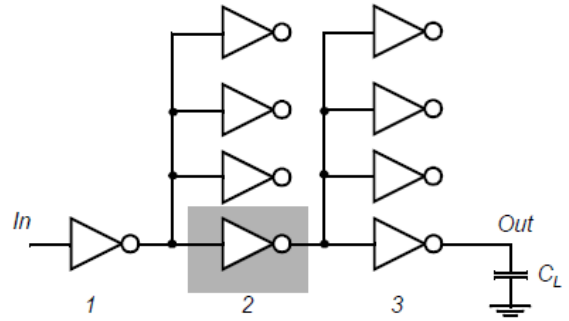
- An ageing model based on critical path delay variations



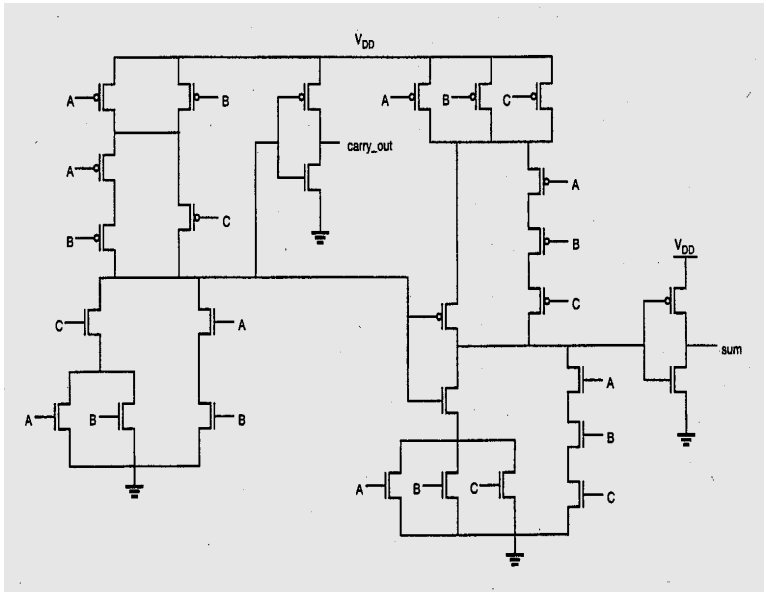
Critical Path Delay Estimation



Memory
(SRAM cell)



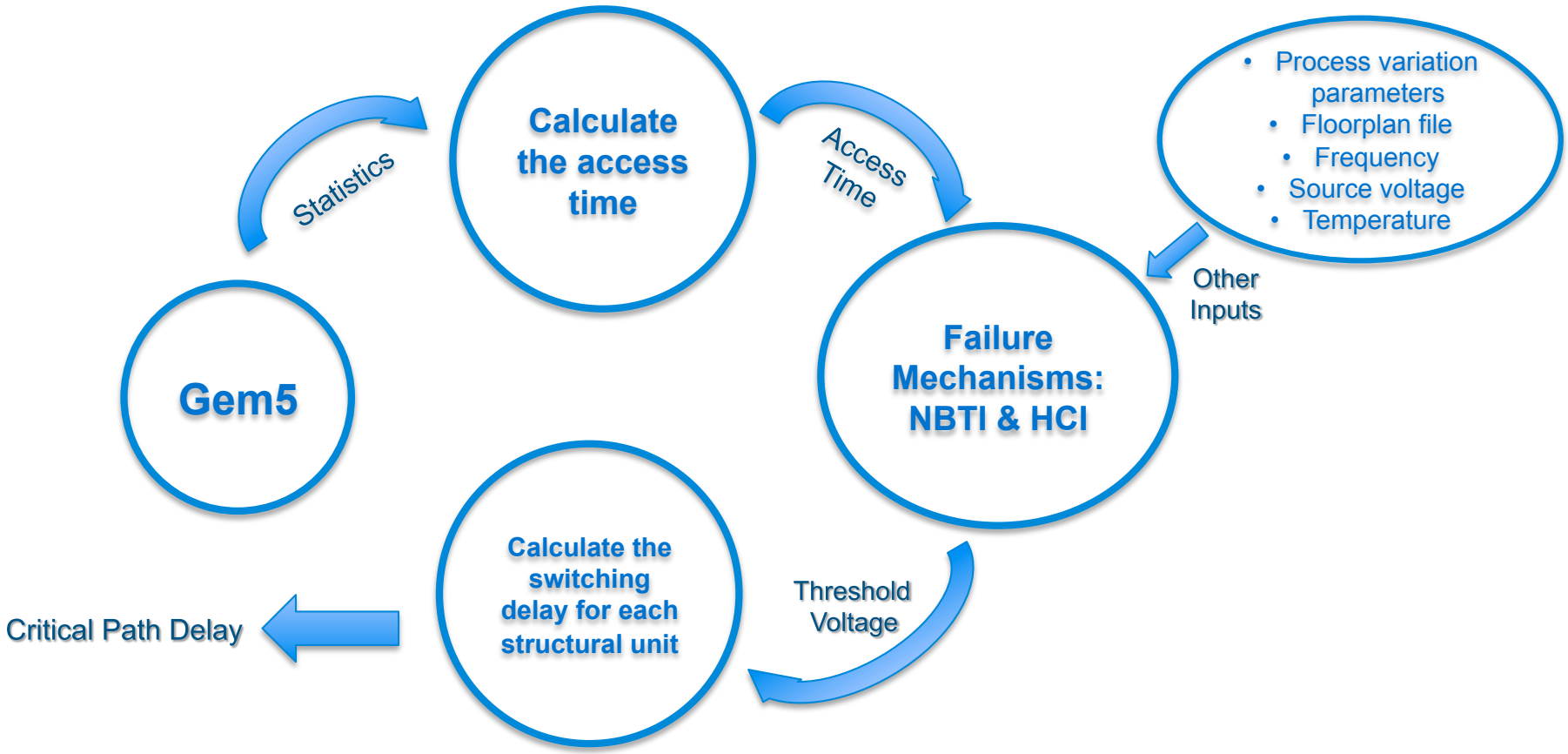
Delay of FO4



Logic
(Full Adder)

$$T_s \propto \frac{V_{dd} L_{eff}}{\mu (V_{dd} - V_t)^{\alpha}}$$

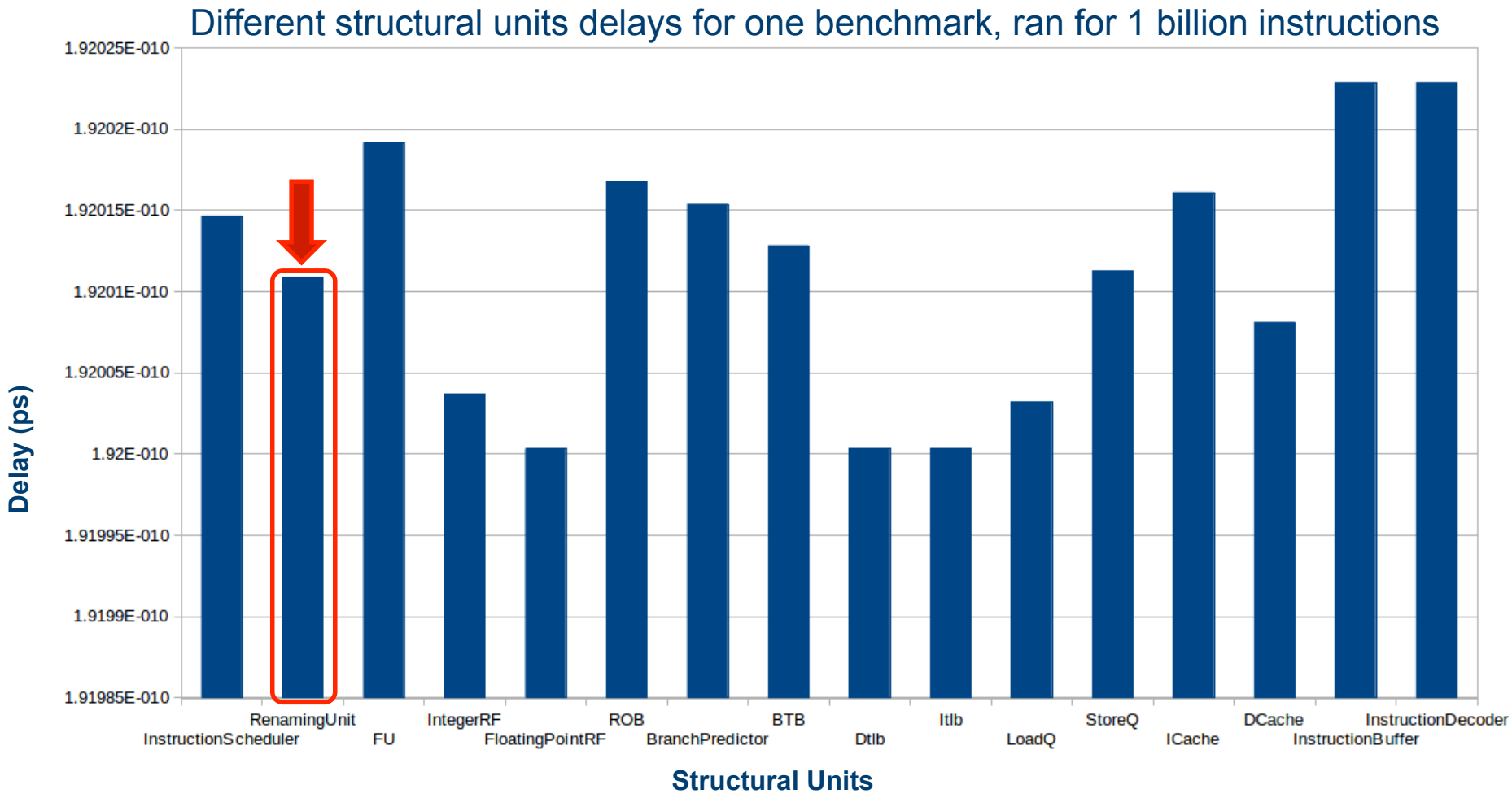
PAM: a Processor Ageing Model



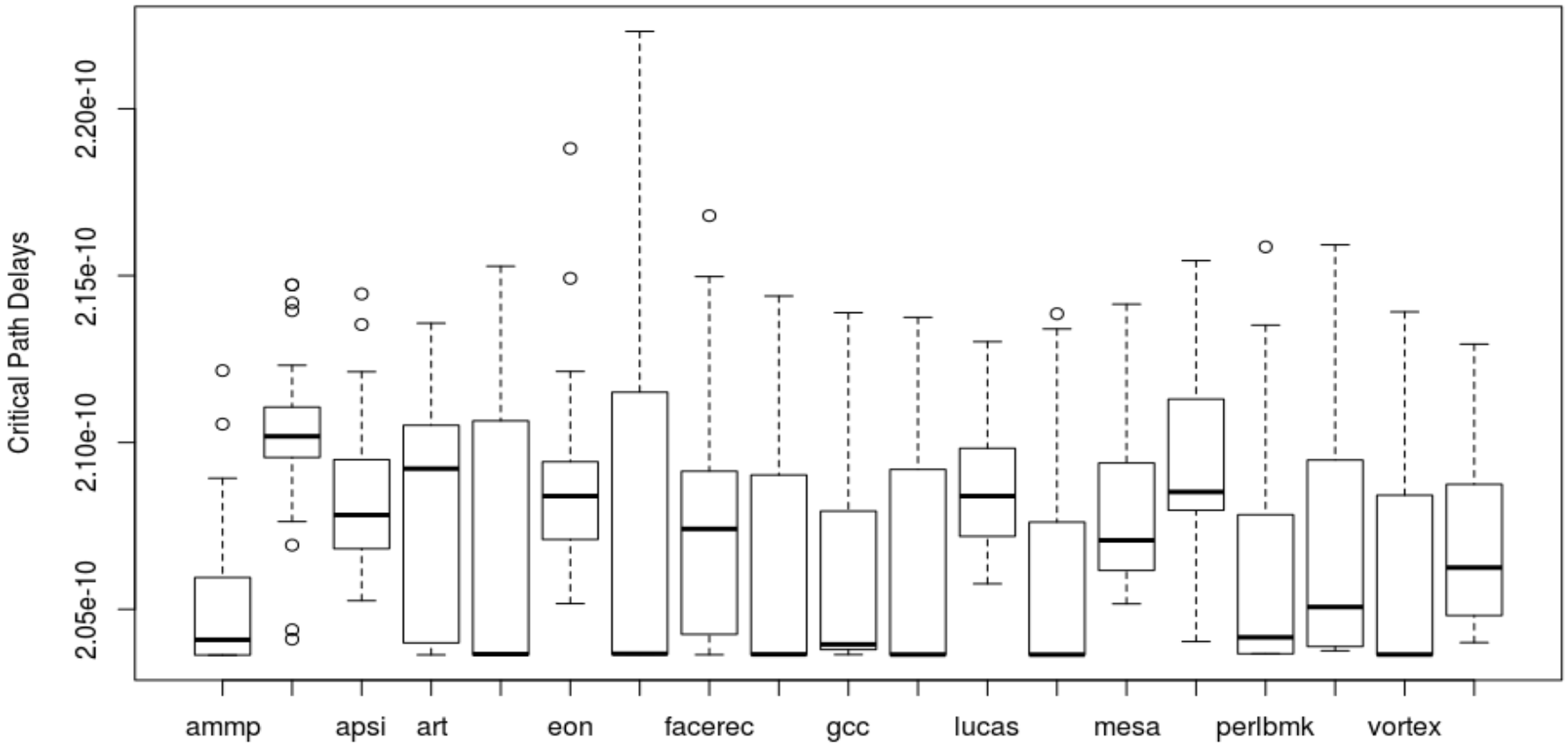
Simulation Environment

- Technology parameters
  - Process technology = 32nm
  - V_{dd} = 1.0 V
  - Frequency = 2.0 GHz
- Single out of Order ARM v7 core
- Ageing Parameters
  - Temperature = 80^{o}C
  - V_{th0} = 200mV
  - Oxide thickness = 0.65 nm
  - Effective gate length = 17nm
- Gem5 Simulator
- SPECCPU 2000 Benchmarks
- VARIUS Framework

Results

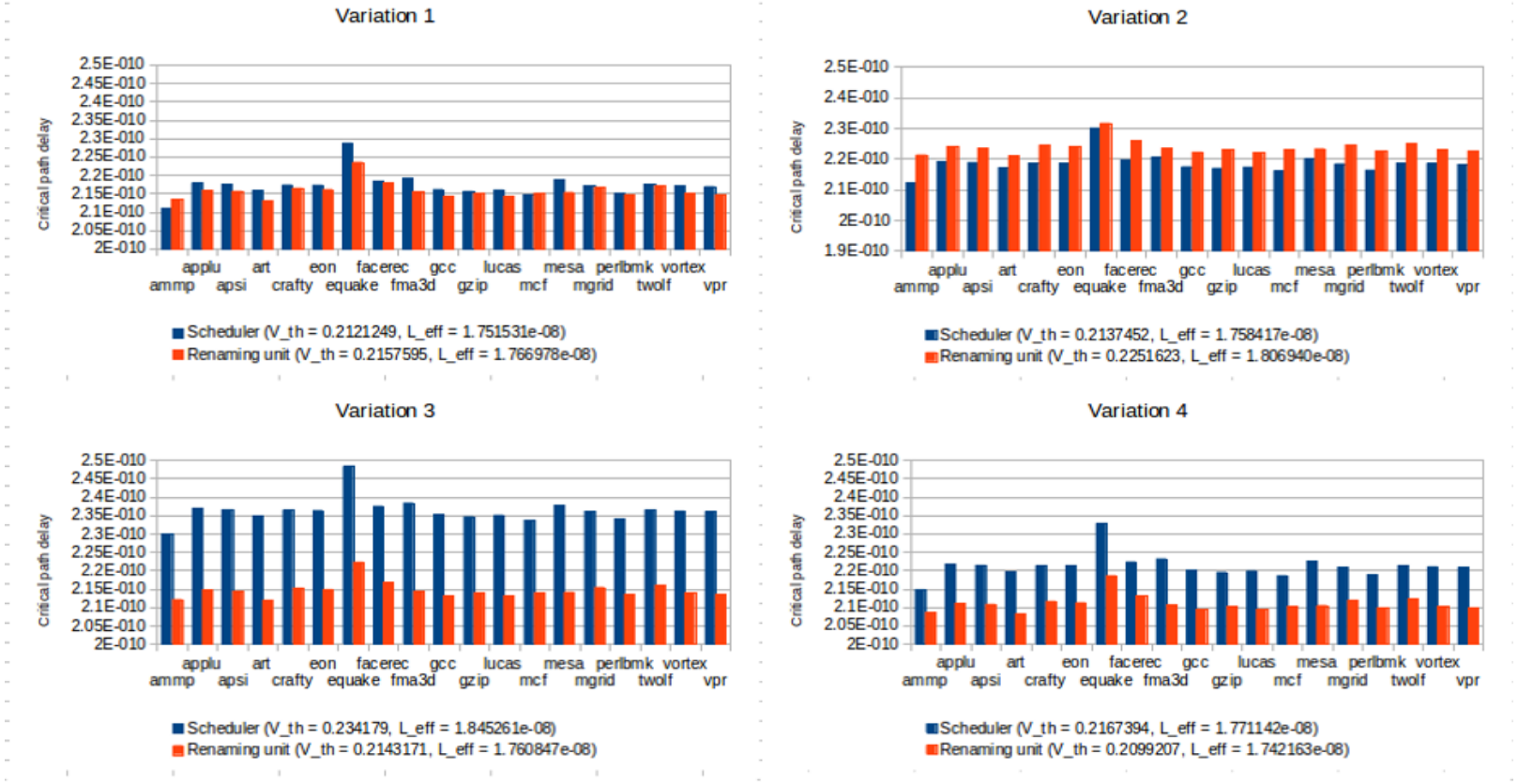

Different structural units delays for one benchmark, ran for 1 billion instructions
1.92025E-010
1.9202E-010
1.92015E-010
1.9201E-010
1.92005E-010
1.92E-010
1.91995E-010
1.9199E-010
1.91985E-010
Delay (ps)
InstructionScheduler
RenamingUnit
FU
IntegerRF
FloatingPointRF
ROB
BranchPredictor
BTB
Dtlb
Itlb
LoadQ
StoreQ
ICache
DCache
InstructionBuffer
InstructionDecoder
Structural Units

Results



Architectural Registers delay within ***Renaming Unit*** for all SPEC2000 benchmarks, ran for 1 billion instructions

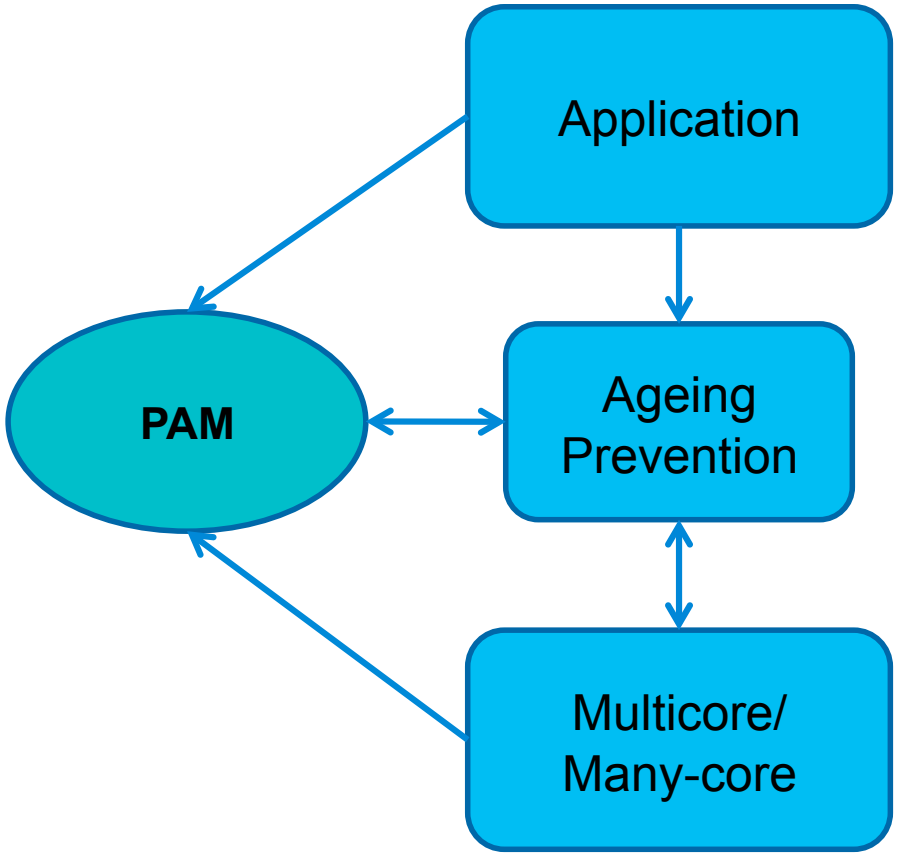
Results



Comparison of the maximum critical path delays for 10 different initial variations, ran for SPEC2000 benchmarks and for 1 billion instructions

Summary

- Micro-Architectural ageing model
- Online mechanism giving state of processor's age
- Characterising the ageing due to applications' behaviour



Future Work

- Transistor level model
- Add more failure mechanisms (EM, TDDB, RTN, etc.)
- Combat processor ageing
  - Compiler techniques (JIT environment)
    - Scheduling
    - DVFS
  - Code restructuring and algorithm selection
  - Create a heterogeneous CMP with “hot spares”

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Thank you

Questions Please?

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Project webpage:
http://www.cl.cam.ac.uk/research/comparch/research/dome.html