Device-Technology Co-Optimisation (DTCO) in the Presence of Acute Variability

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Summary

- Introduction
- 22nm FinFETs: *the Intel benchmark*
- 14nm FinFETs: *Interplay between process and statistical variability*
- 10nm FinFETs: *Si vs. Ge*
- 7nm FinFETs: *the role of III-Vs*
- Conclusions

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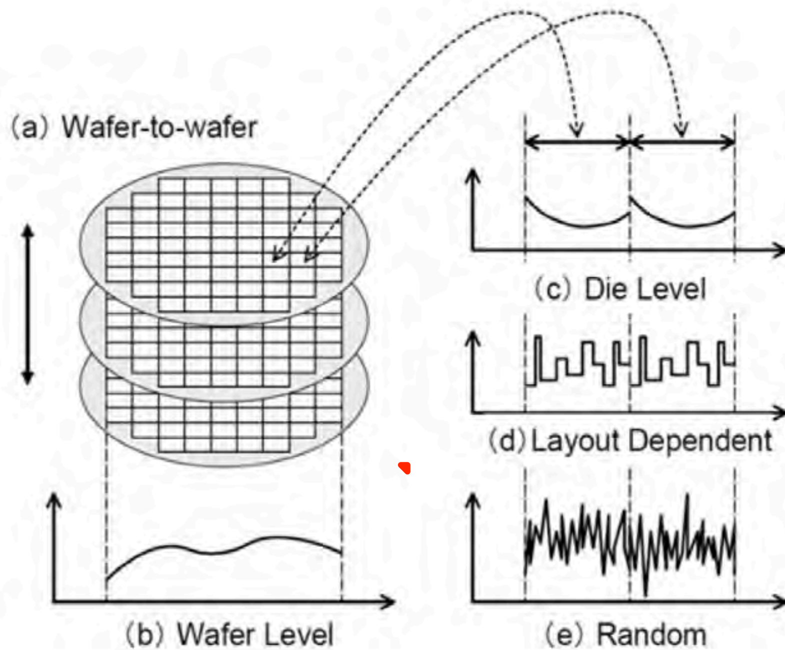
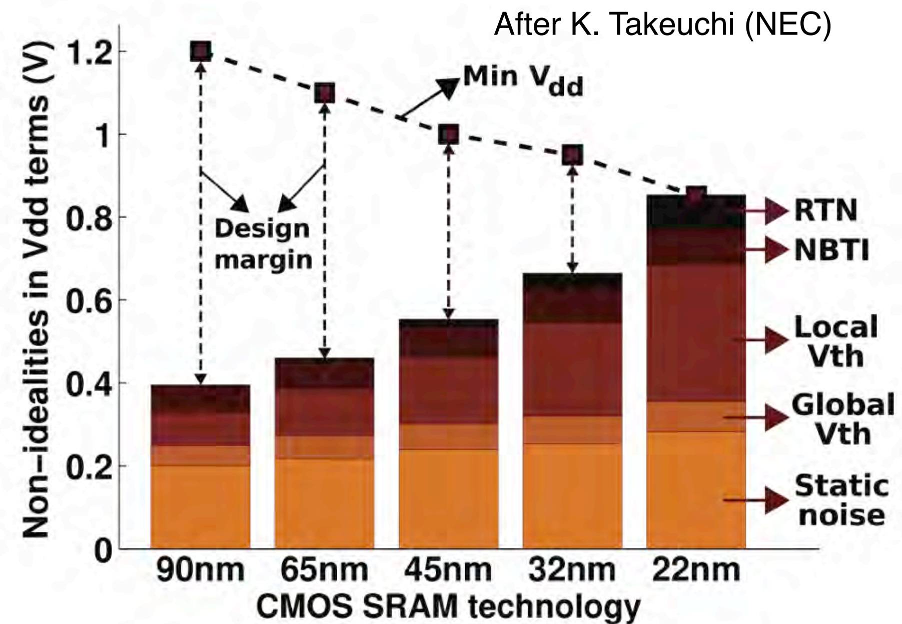
Statistical variability is one of the major challenges associated with scaling

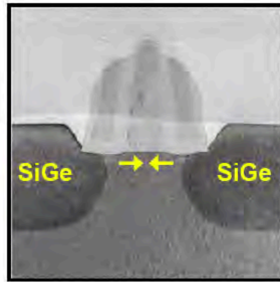


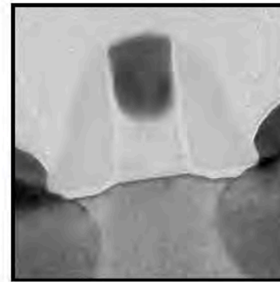
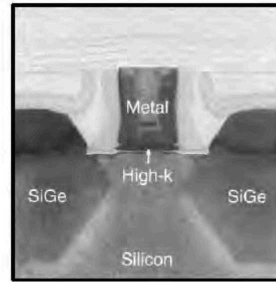


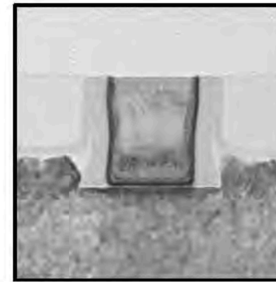
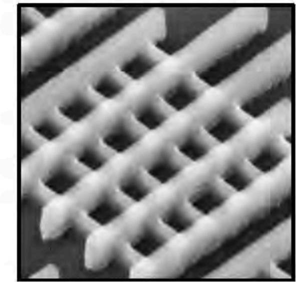
Variability results in higher parametric yield loss

Saturation in performance and increasing variability drives the CMOS innovations

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm



Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

M Bohr (Intel)

Strained Silicon

High-k Metal Gate

Tri-Gate

FinFETs improve performance and can reduce statistical variability

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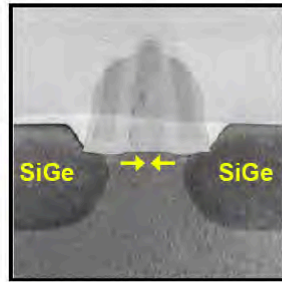
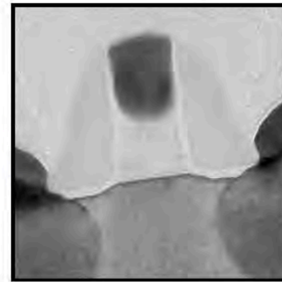
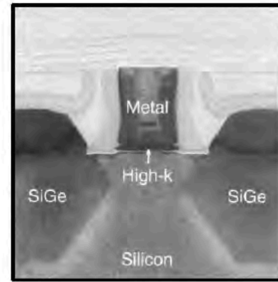
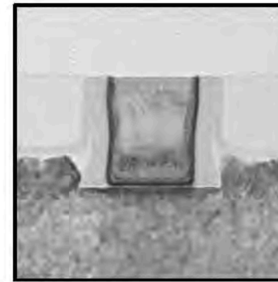
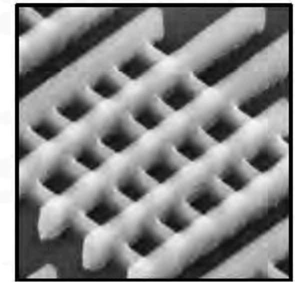










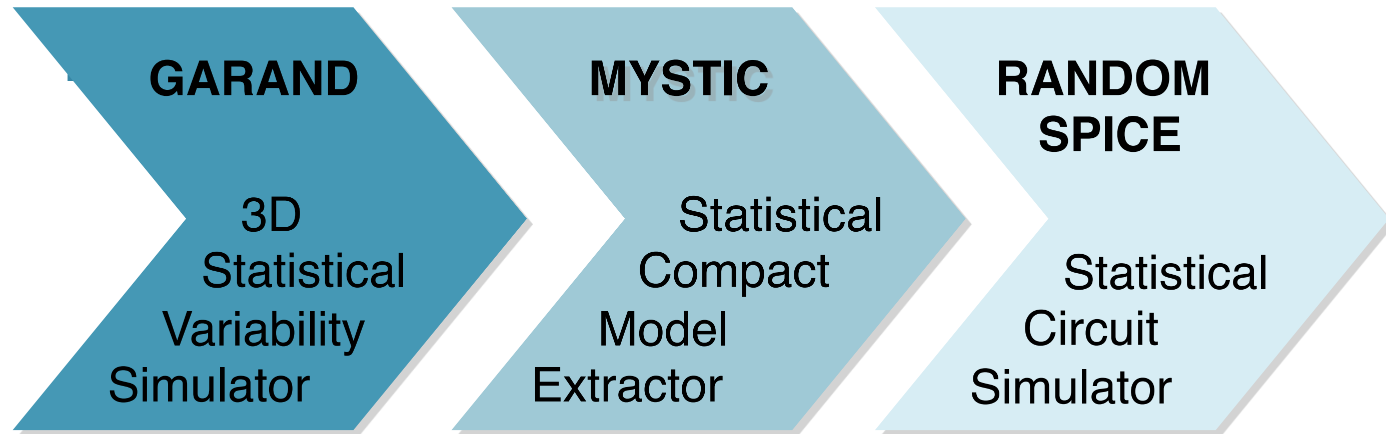
$$\sigma \Delta V_T = A_V / \sqrt{WL}$$

$$A_V \sim t_{ox} N_{A(D)}^{0.4}$$

- Circuits have to be adjusted/optimized for the specific behavior of new devices.
- Technology/Devices should be optimized for specific circuit requirements.
- The early stages of DTCO is based on TCAD/CM/ Circuit simulations.
- Requires seamless link between TCAD and circuit simulation.
- Reduces dramatically time to market.

DTCO – critical in advanced CMOS technology

The GSS Tool Suite that enable the Flow



- Drift diffusion, Monte Carlo (NEGF) modules.
- Multiple variability sources
- Random discrete dopants
- Line edge roughness
- Gate stack granularity
- Trapped discrete charges
- Others - custom

- Nom and Stat Models
- Multiple stat parameters
- Supports PCA and NPM
- High accuracy
- Supports BSIM, PSP and HiSIM

- Frontend for advanced statistical simulation
- Supports ngspice, Eldo and Spectre.
- Supports PCA and NPM.
- Unprecedented SRAM analysis accuracy.
- Performance/power/yield analysis (PPY)

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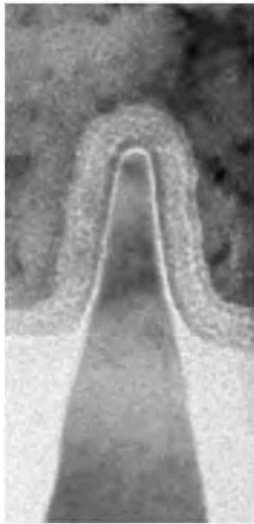
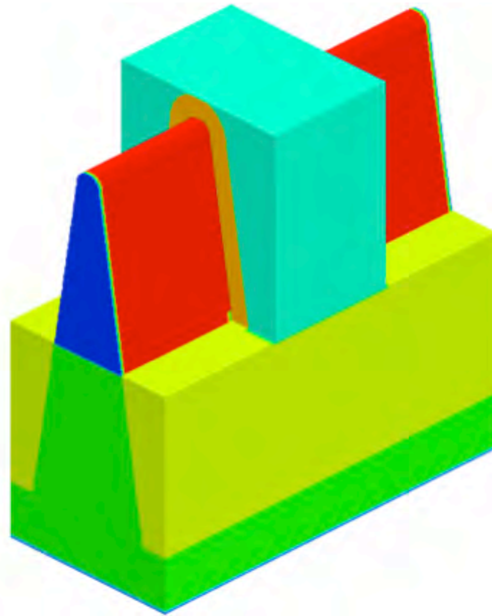
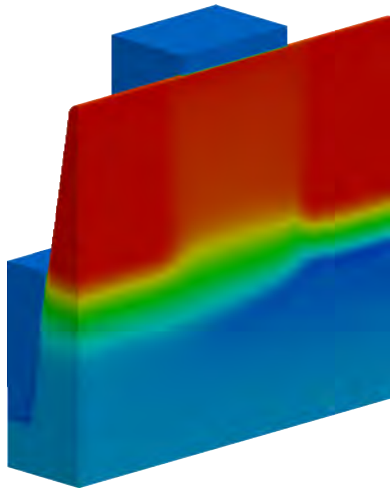
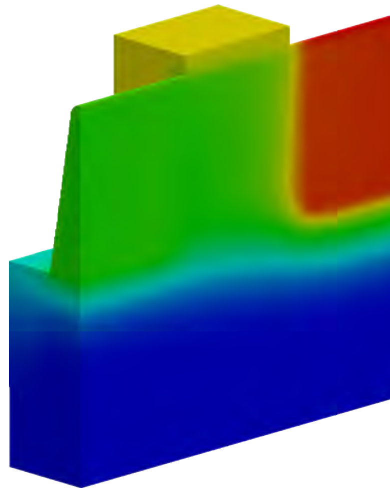
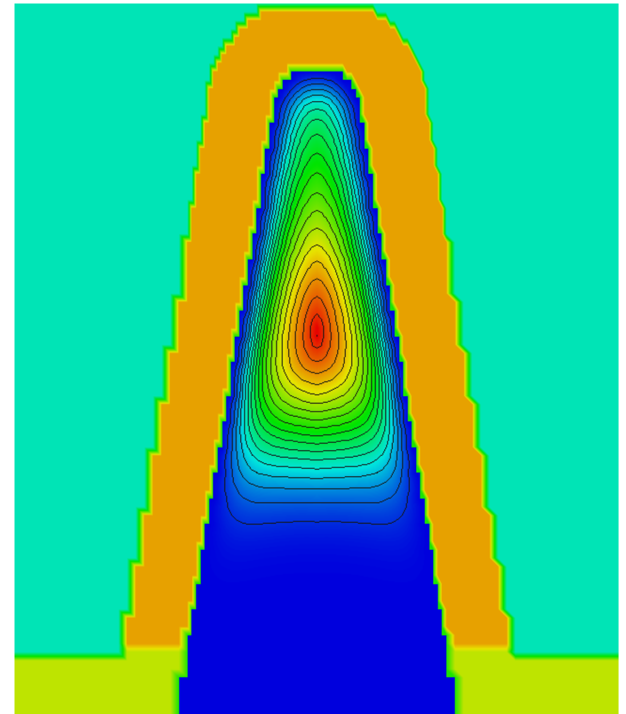
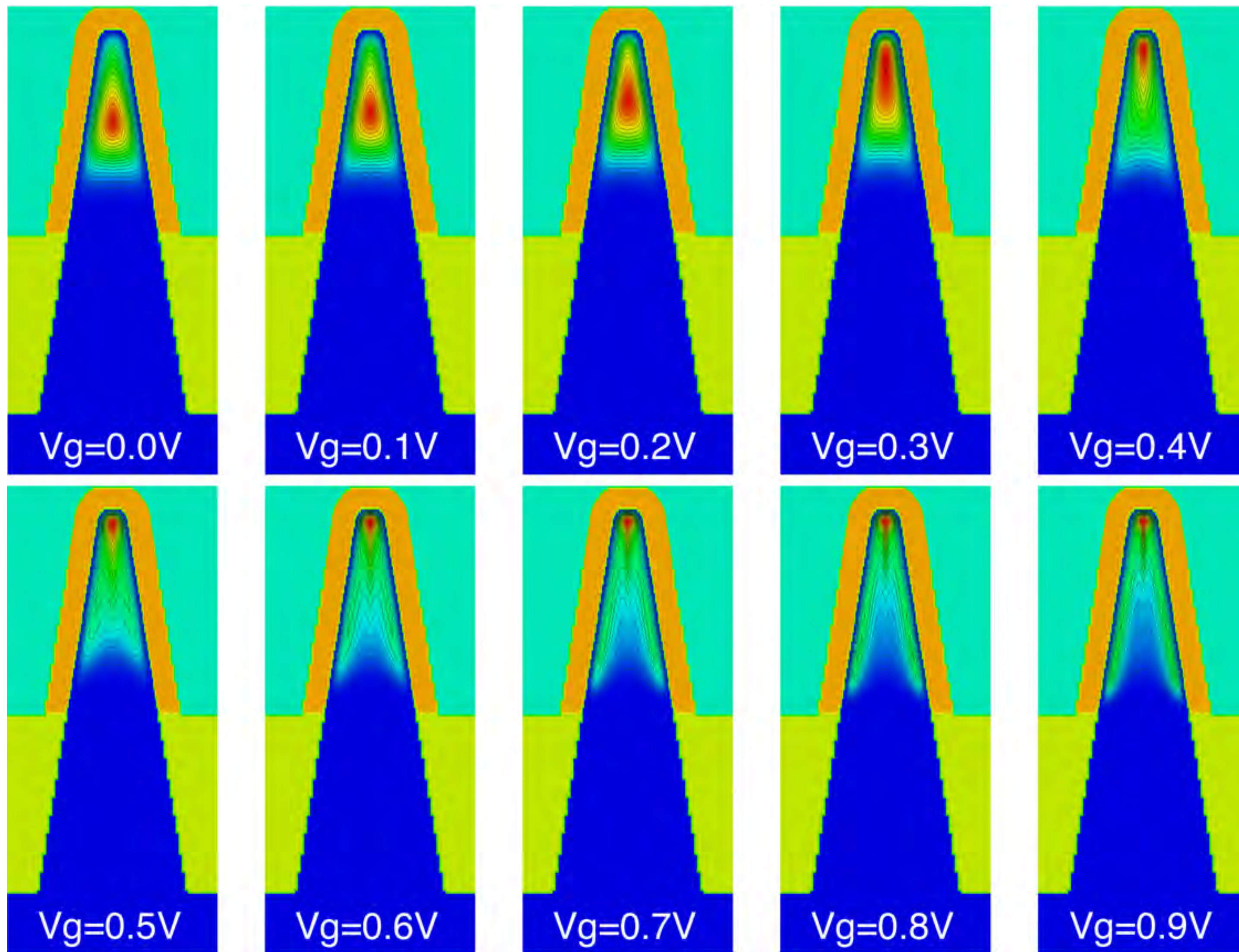
Intel 22nm FinFETs

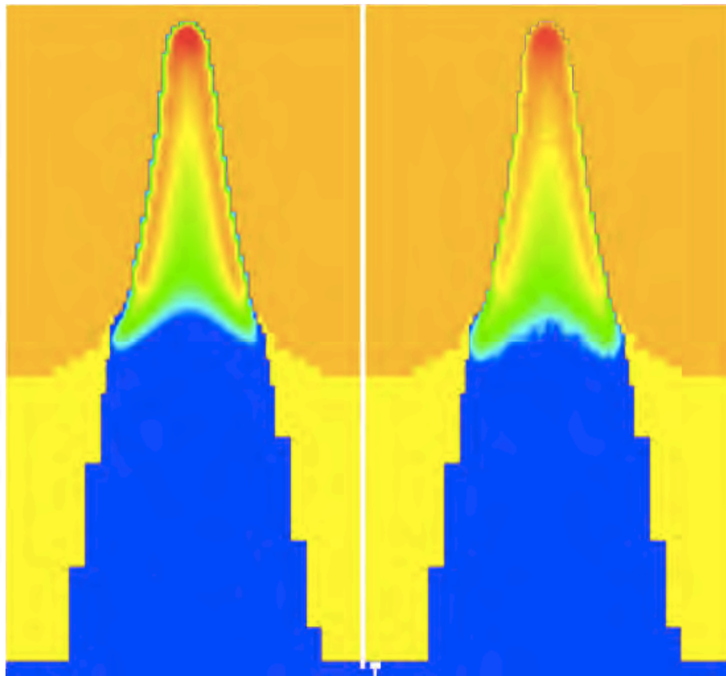
Intel 22nm FinFETs



3D Ensemble MC simulation provide predictability

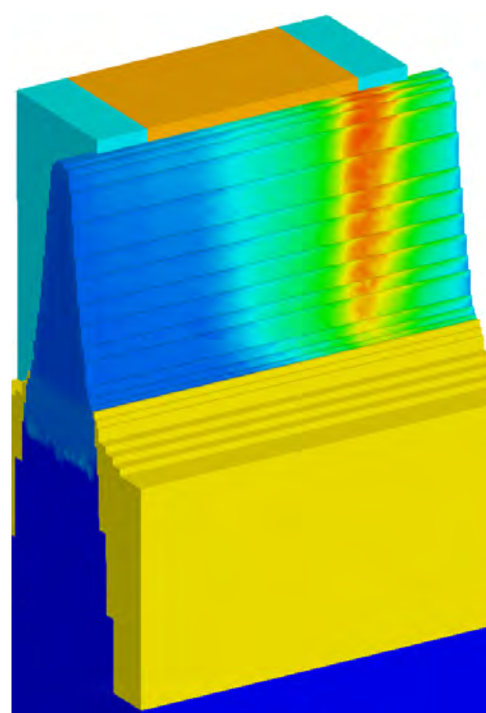
Quantum confinement is important

Non-equilibrium transport is also important

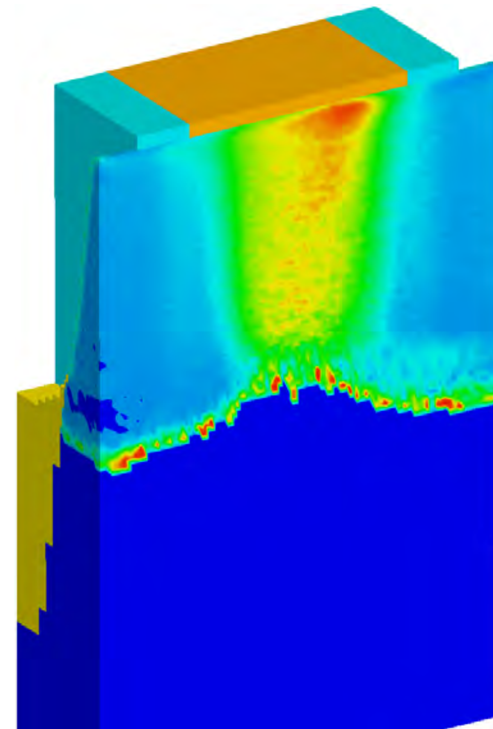


DD

MC

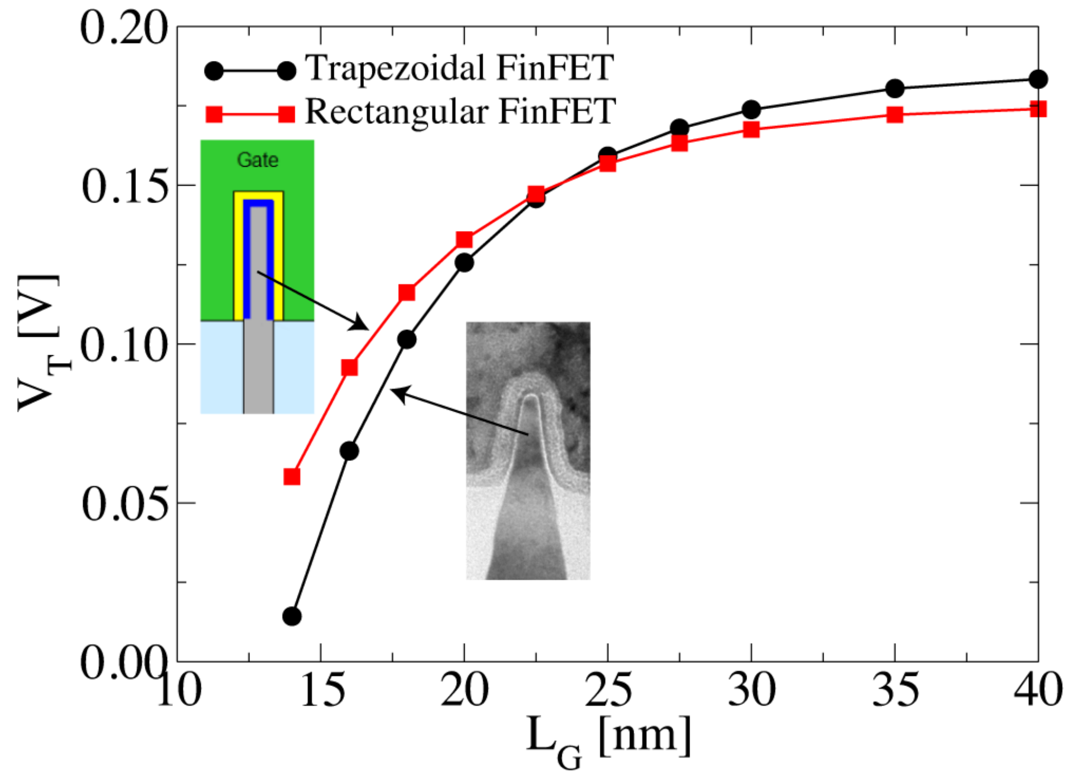


Electron energy

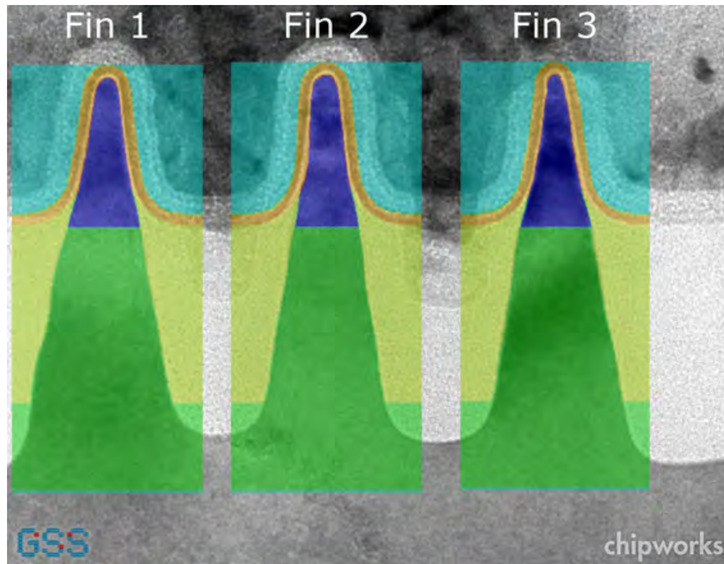


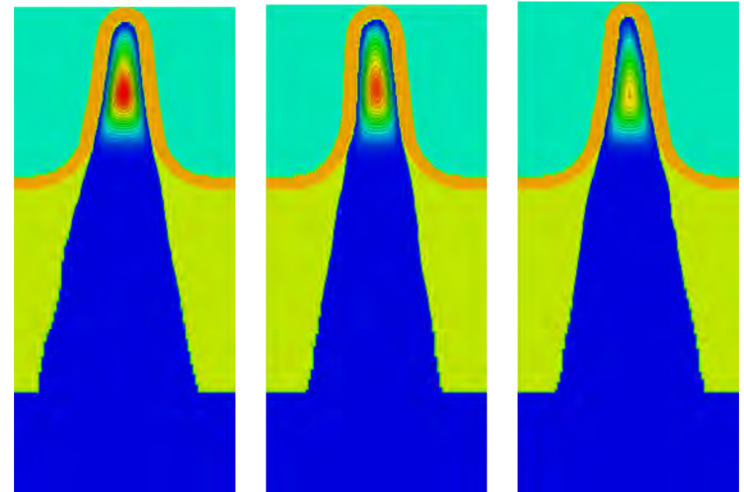
Electron velocity

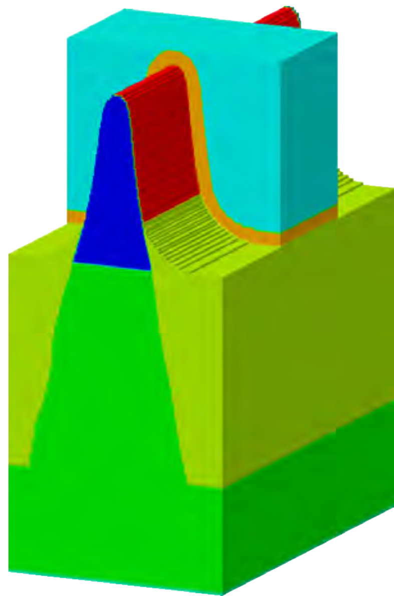
Intel 22nm FinFETs

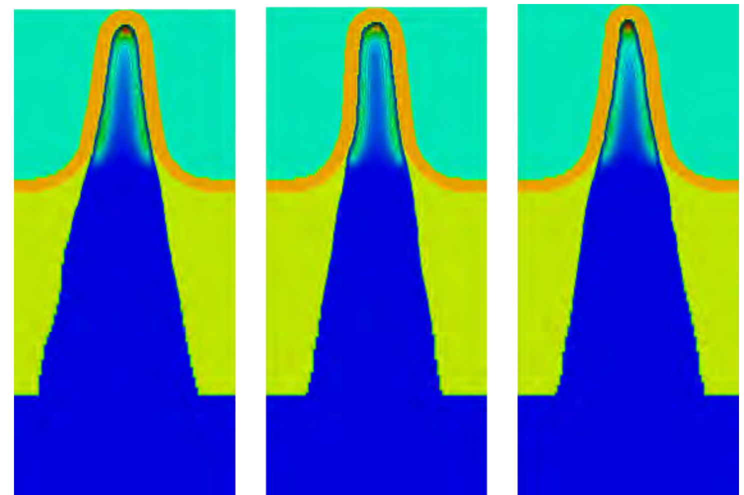


Intel 22nm FinFETs

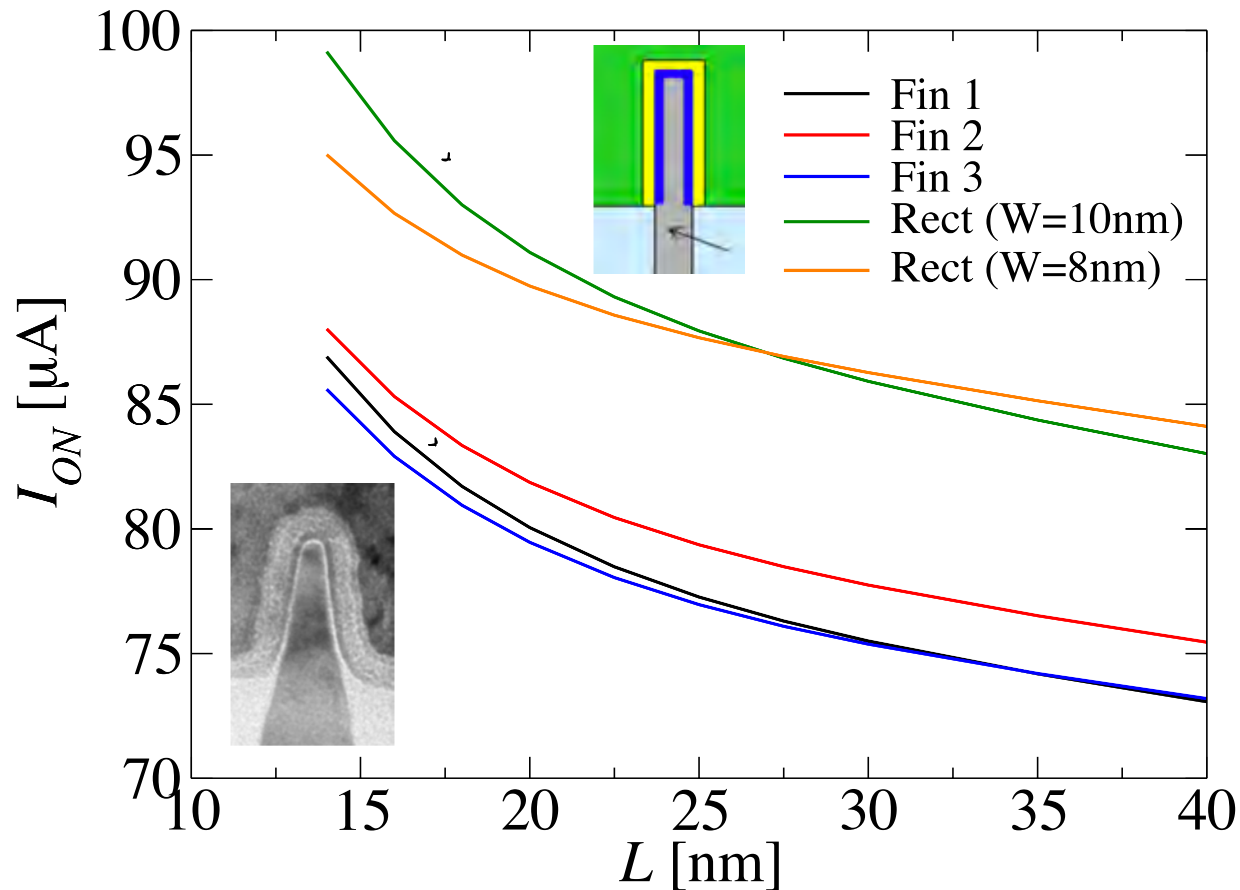






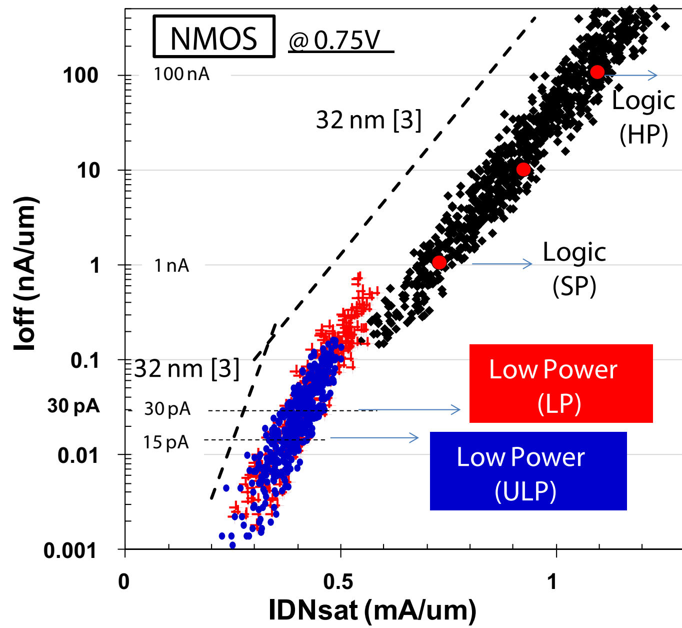


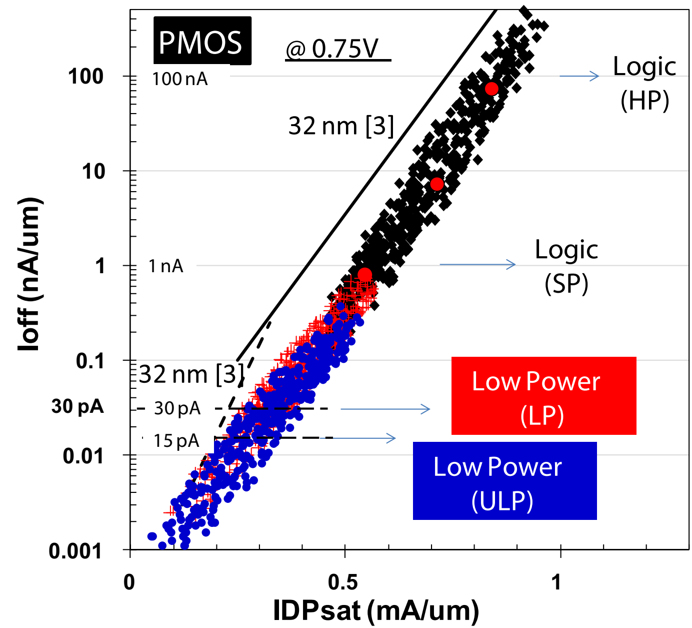
Intel 22nm FinFETs

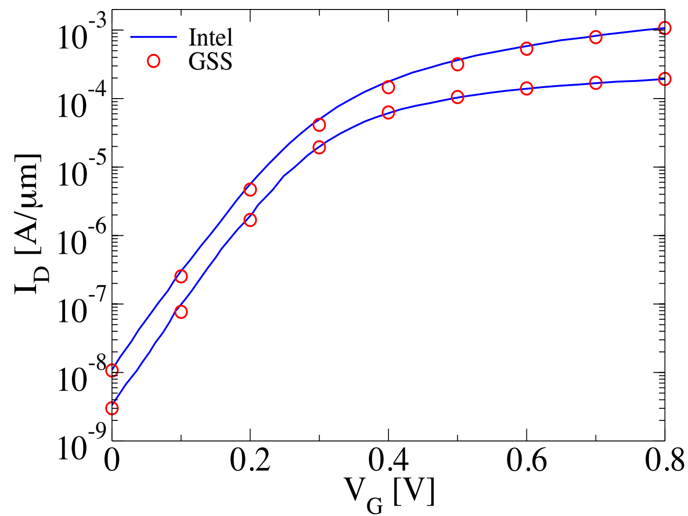


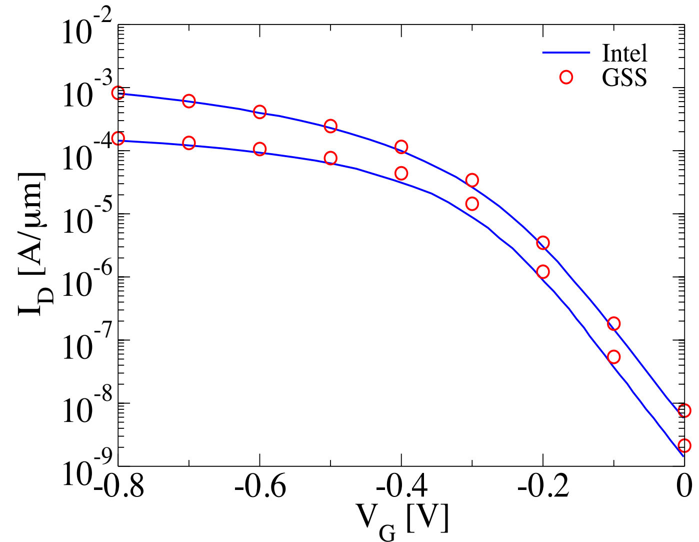
Rectangular fins have 15% higher performance for equivalent width and height.

Intel 22nm FinFETs

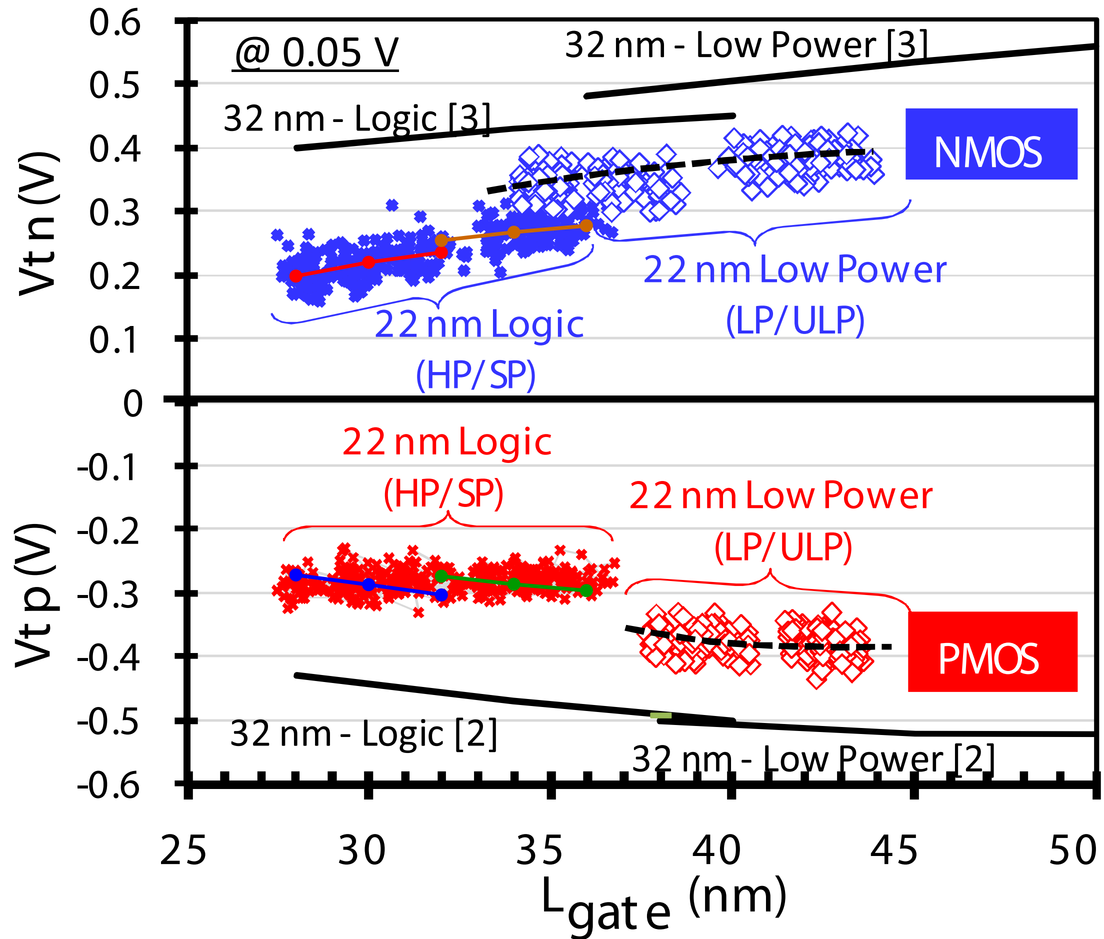








Intel 22nm FinFETs



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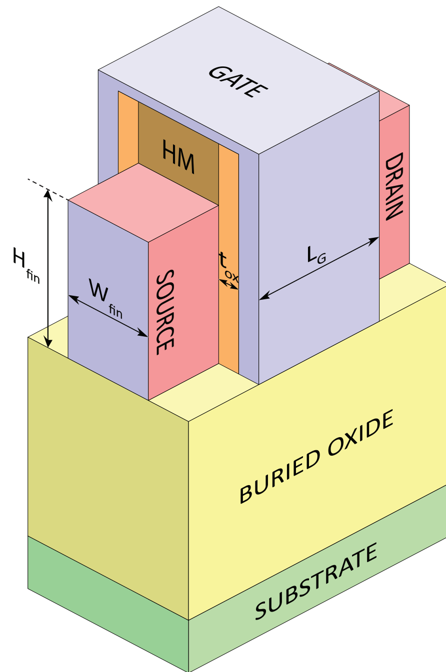
14nm DG FinFET specification

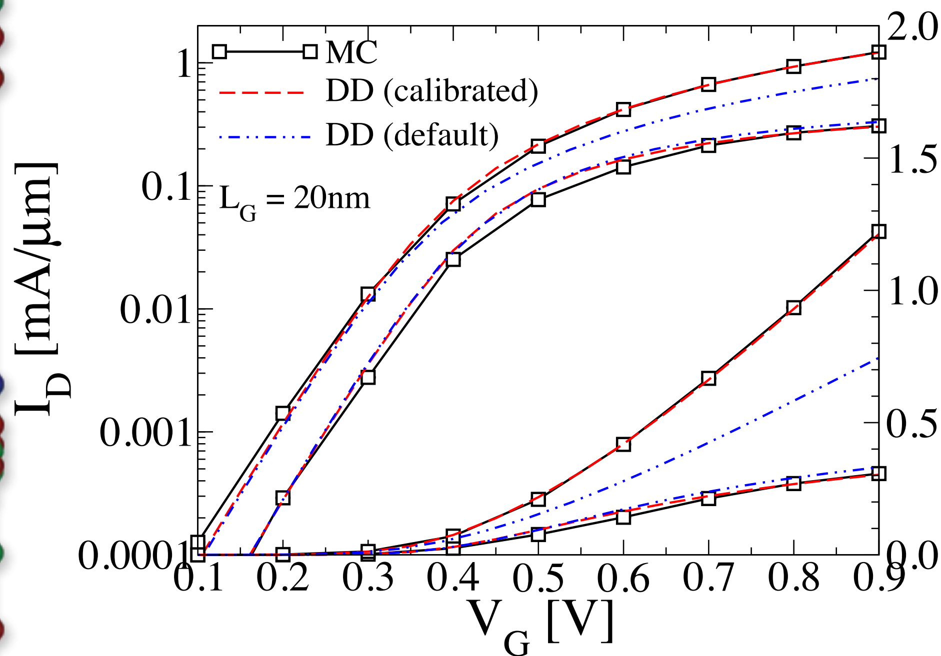


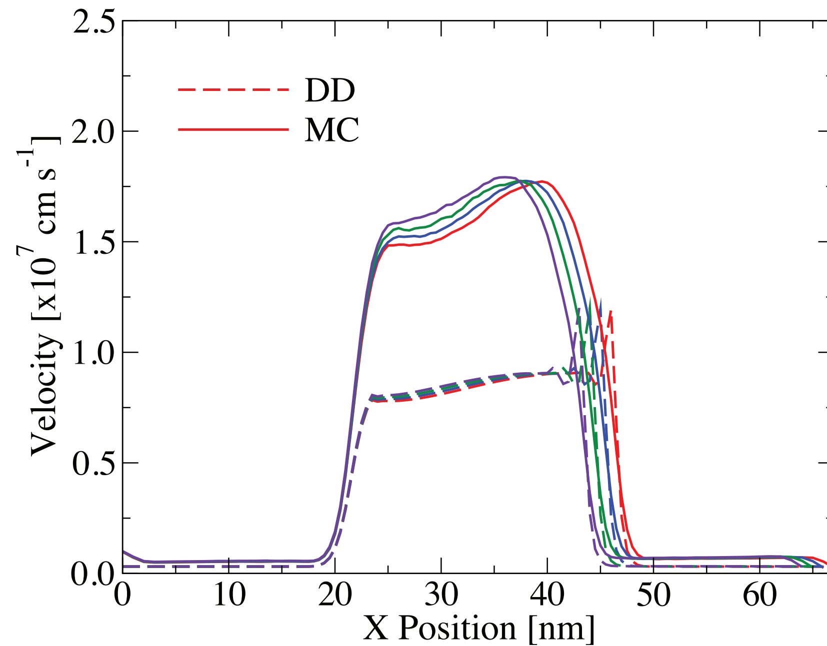
Dimension	Min (nm)	Max (nm)
Fin Width	8	12
Fin Height	22	28
Gate Length	18	22

- Double gate FinFETs targeted at 14nm technology node.
- Devices targeted for high performance SRAM application.
- Process variation aware design.

T=85°C V_{DD} = 0.9V	NMOS	PMOS
I_{ON} (mA/μm)	0.9	0.8
I_{OFF} (nA/μm)	10	10
DIBL(mV/V)	56	65
SS(mV/Dec)	86	88

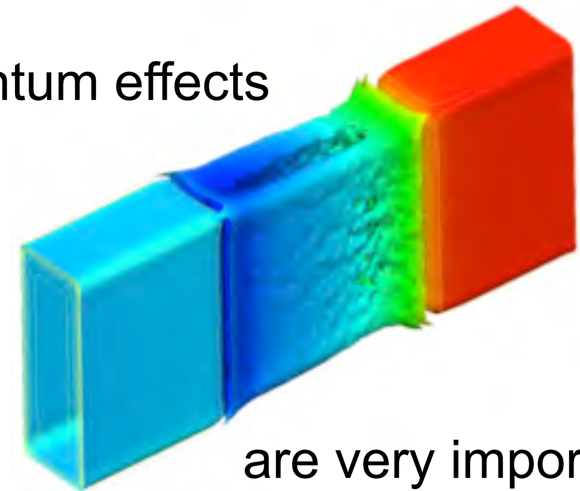
The role of predictive MC simulations





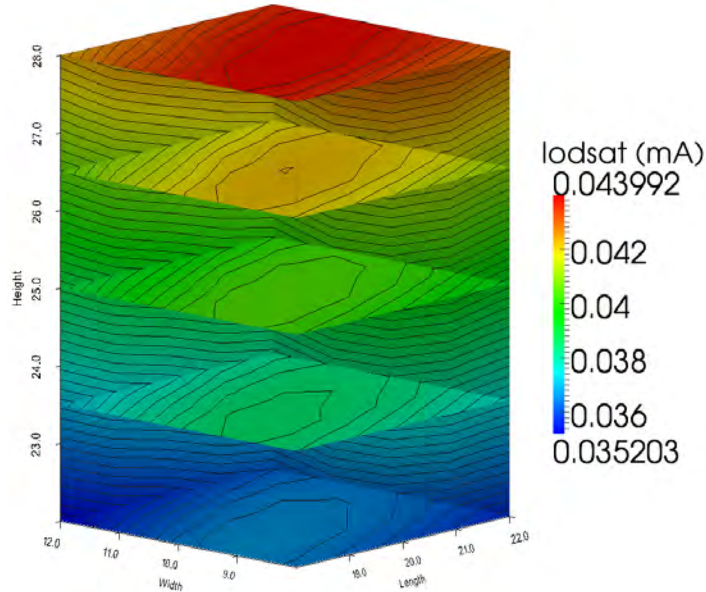
- Only EMC simulations can predict performance.
- Quantum corrections are essential.
- DD simulations can be calibrated to EMC.

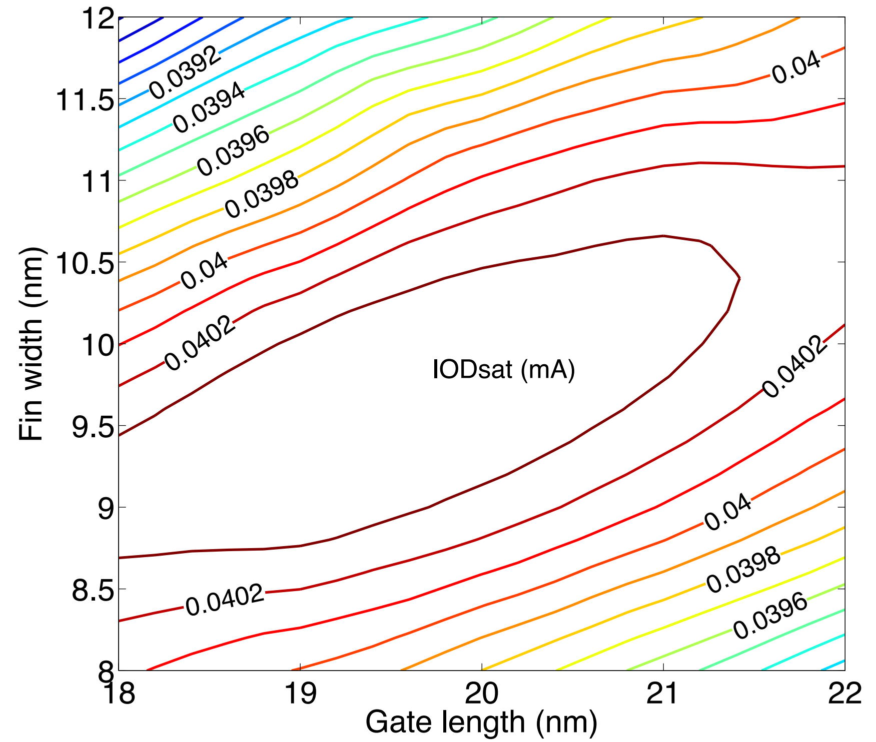
Quantum effects

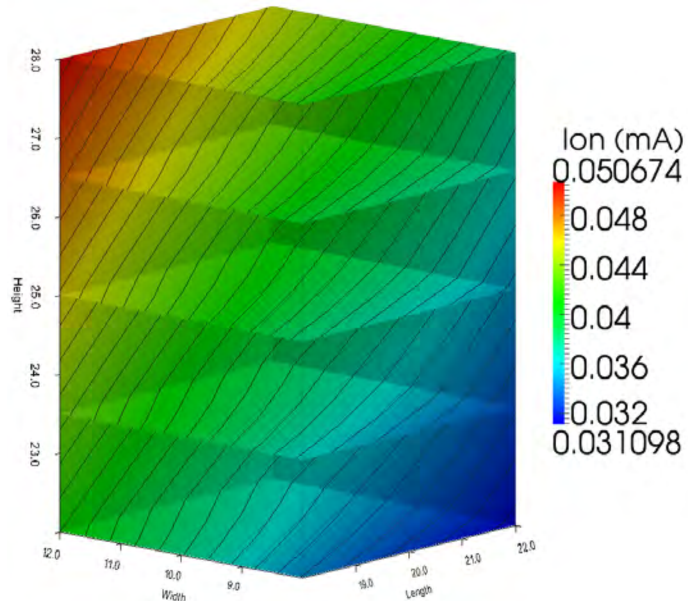


are very important

Process induced variability



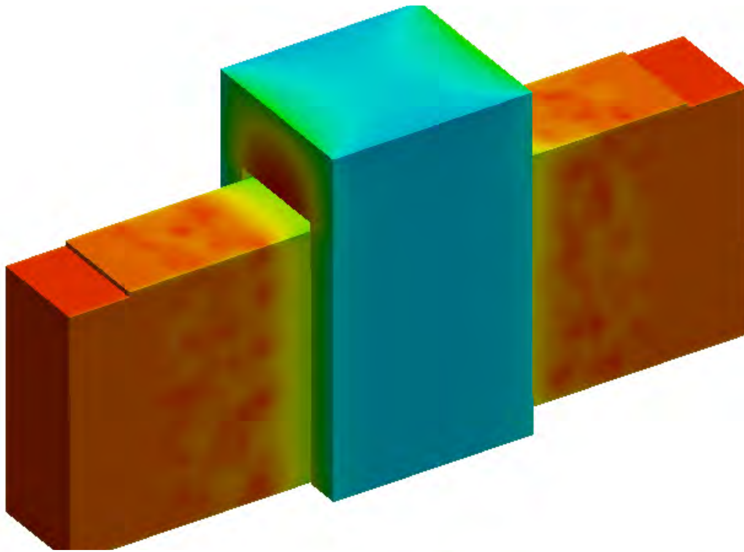




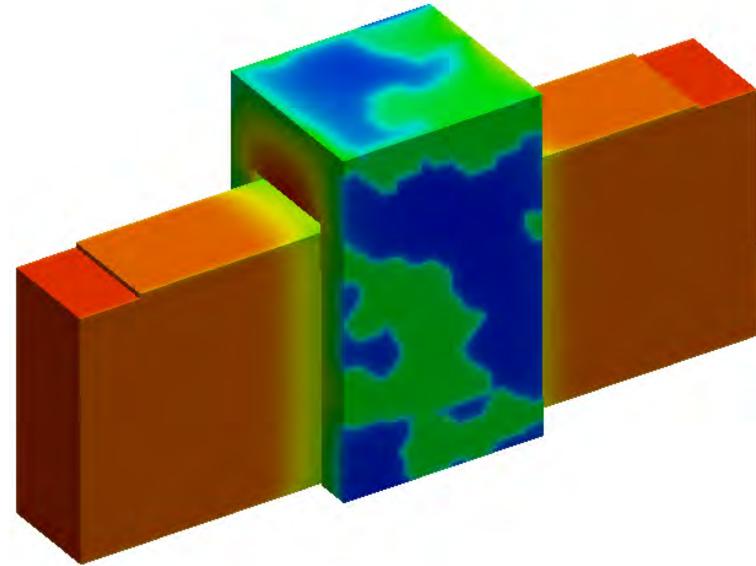
- Captured by experiment design.
- Dependence on L, H_F, W_F, T_{OX}.

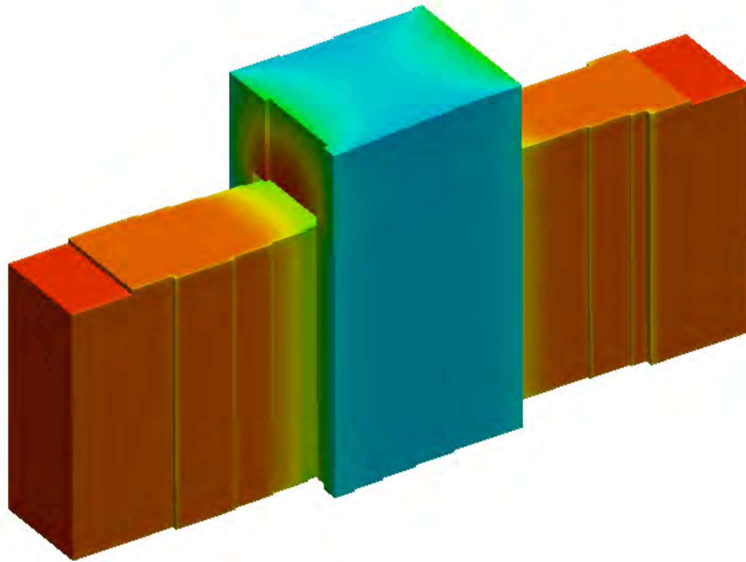
Statistical Variability Simulations

RDD



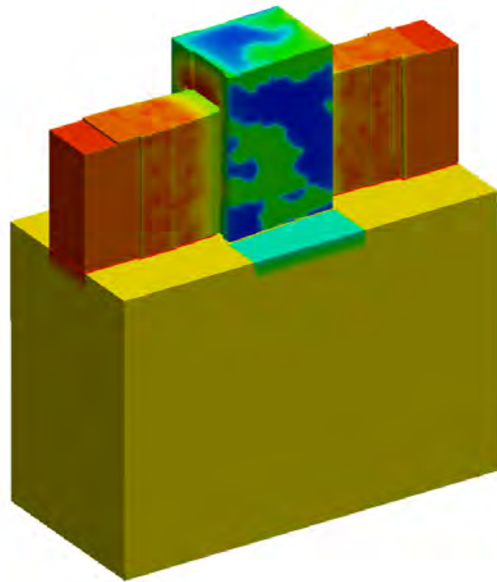
MGG

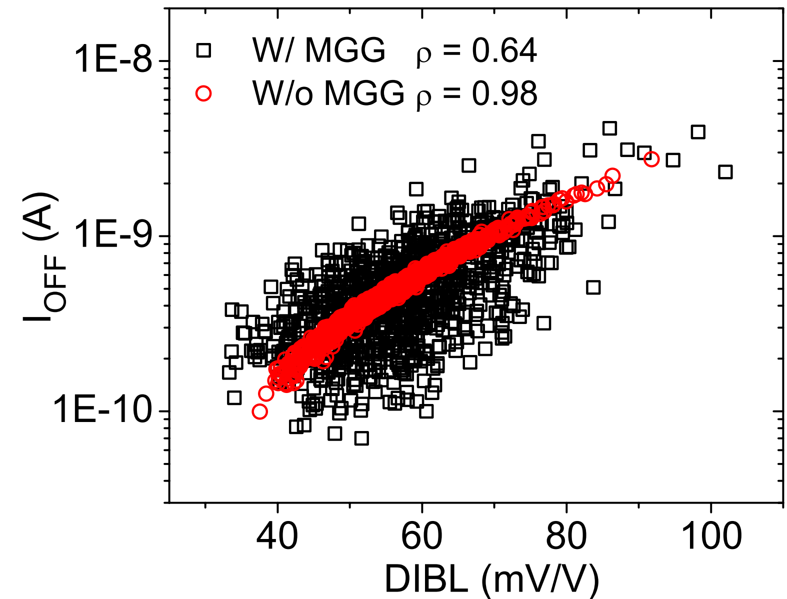


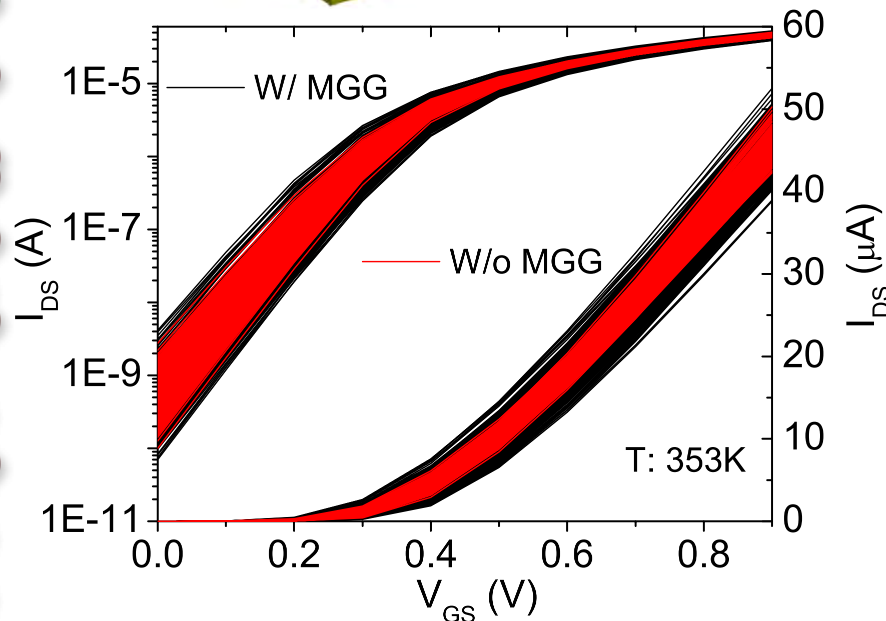


GER+FER

Nominal Device Statistical Variability

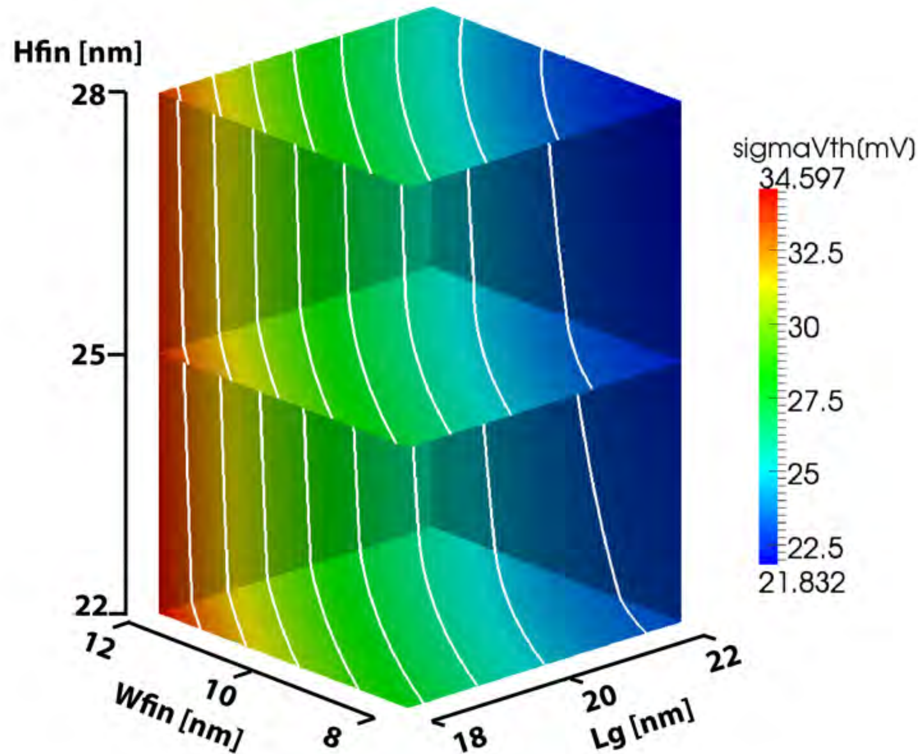


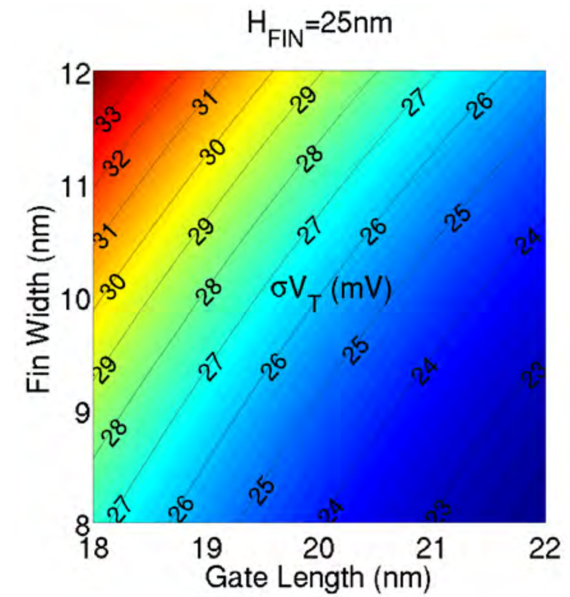


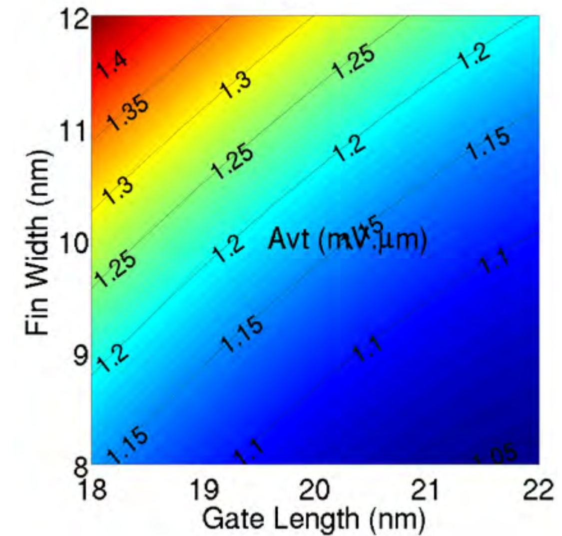


Correlation between subthreshold figure of merits, such as I_{OFF} and DIBL, can be a good indicator to show whether MGG is an active variability source.

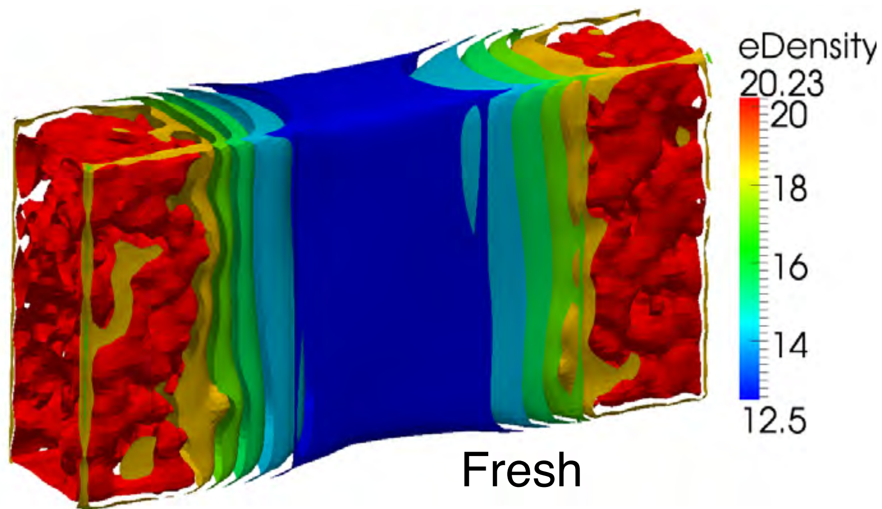
Correlation between process and statistical variability

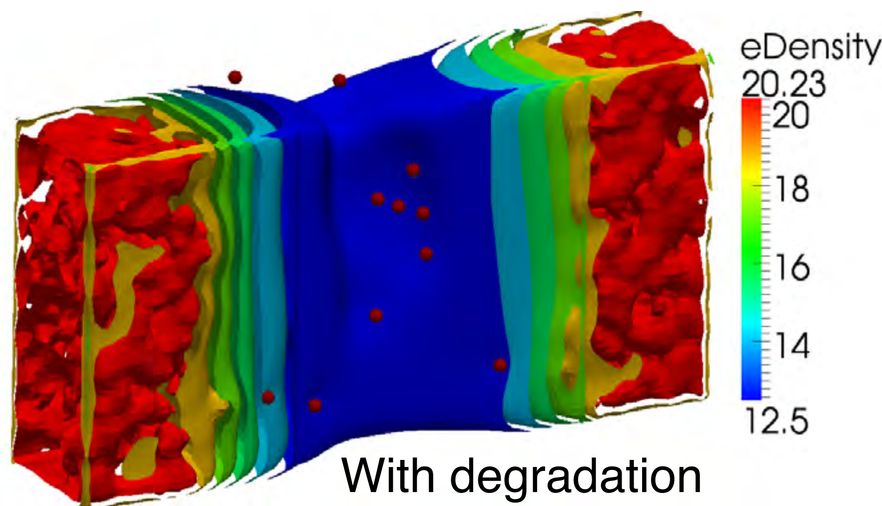


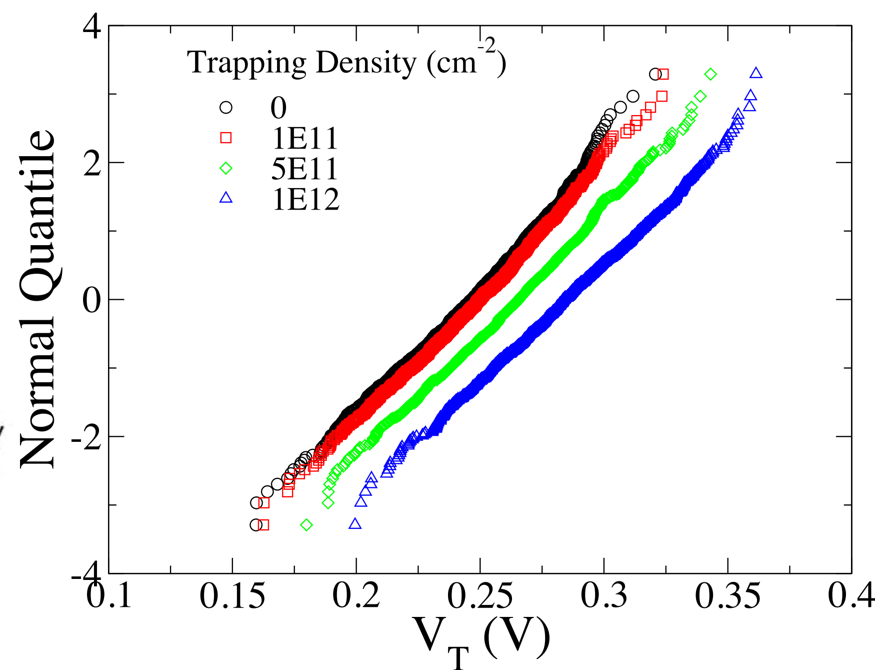




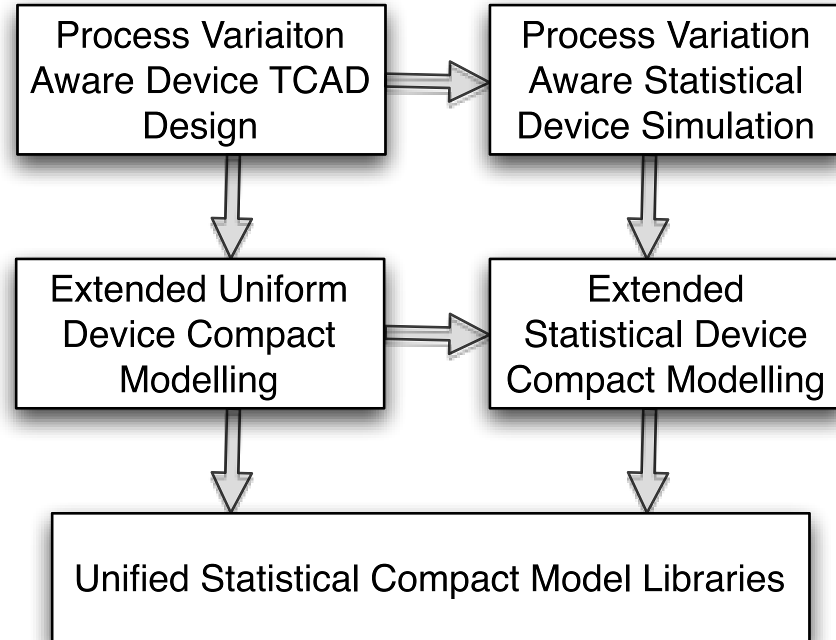
Statistical aspects of Reliability

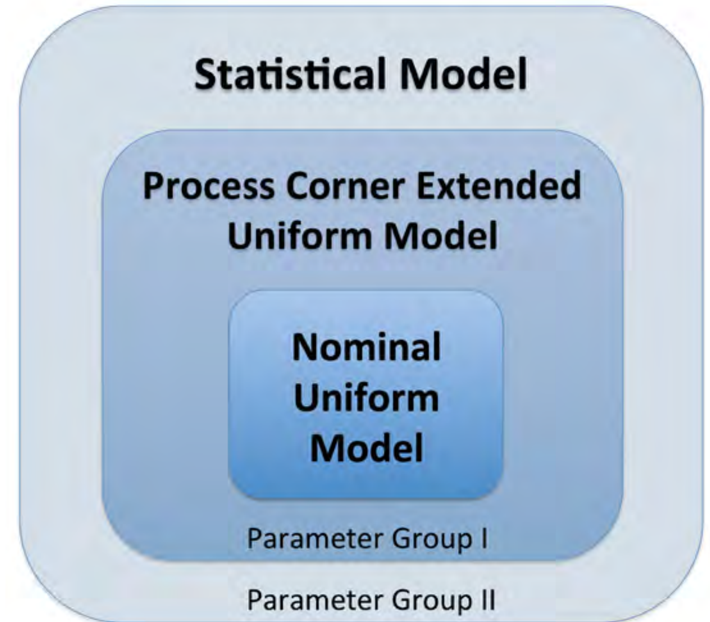




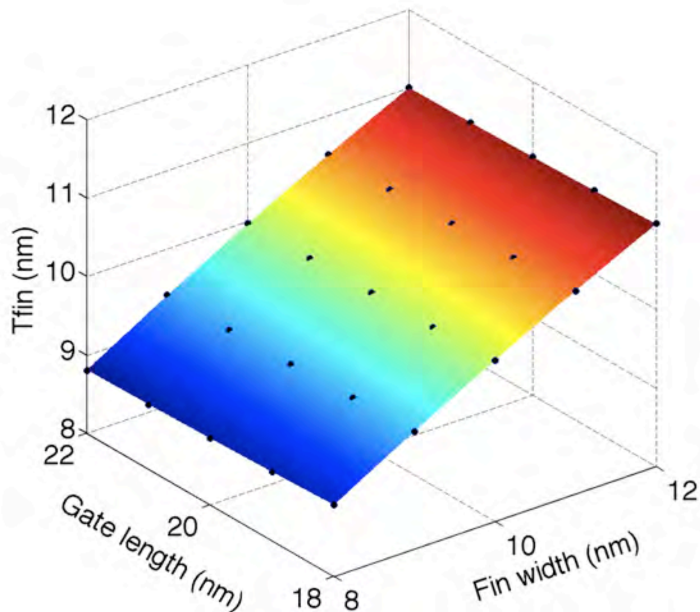


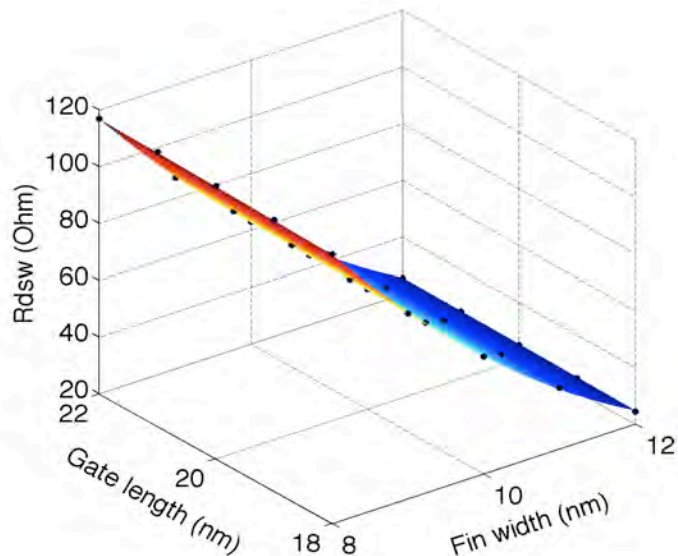
Statistical Compact Modelling Procedure

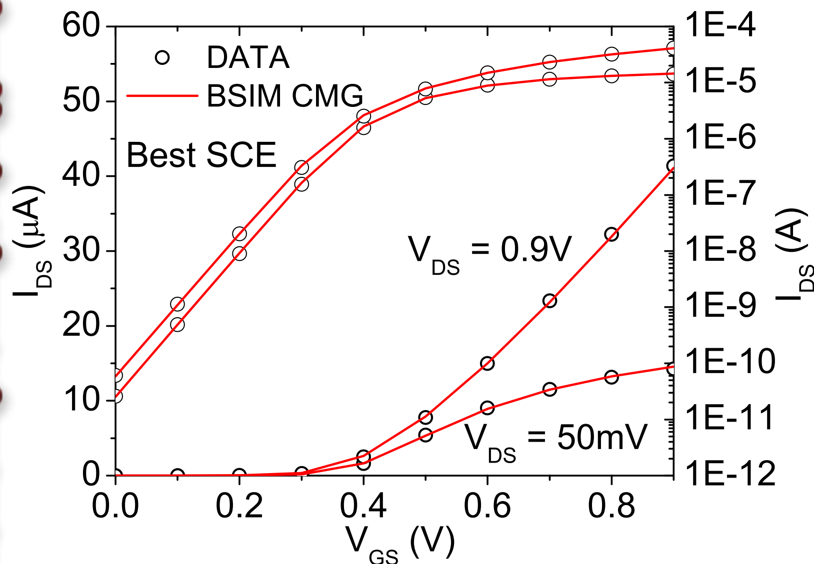


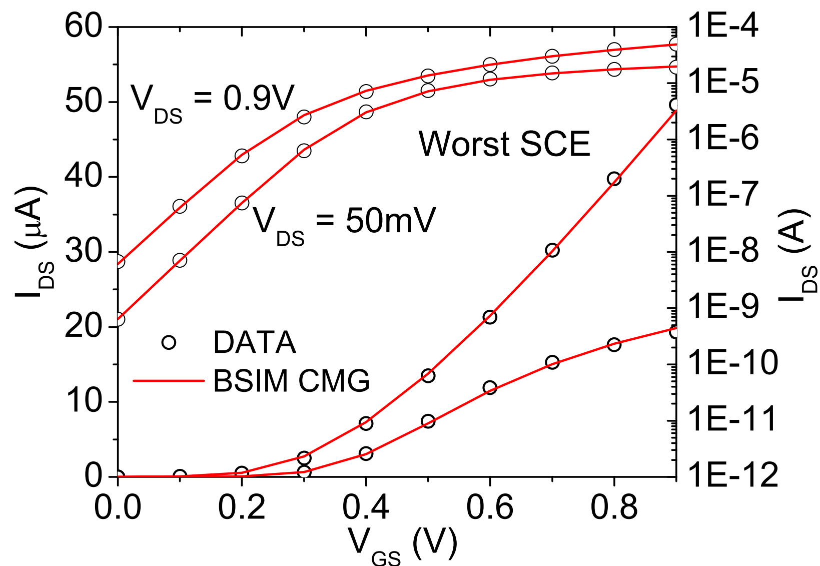


Extended Uniform Model – Group 1 Parameter

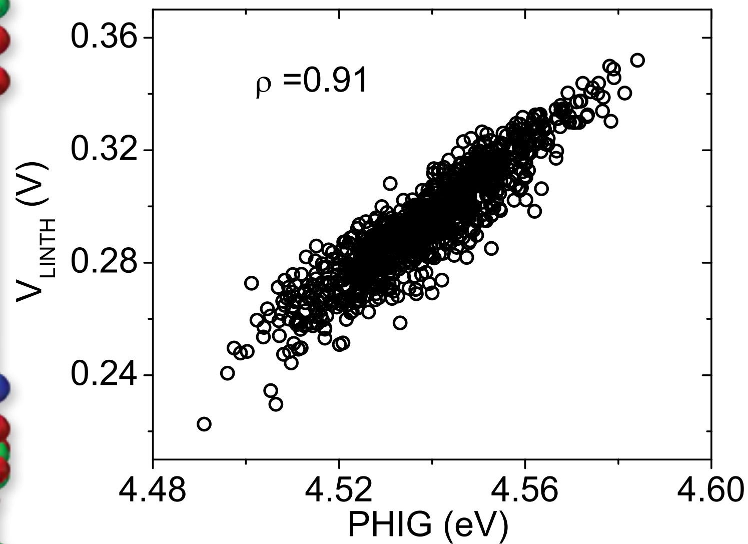


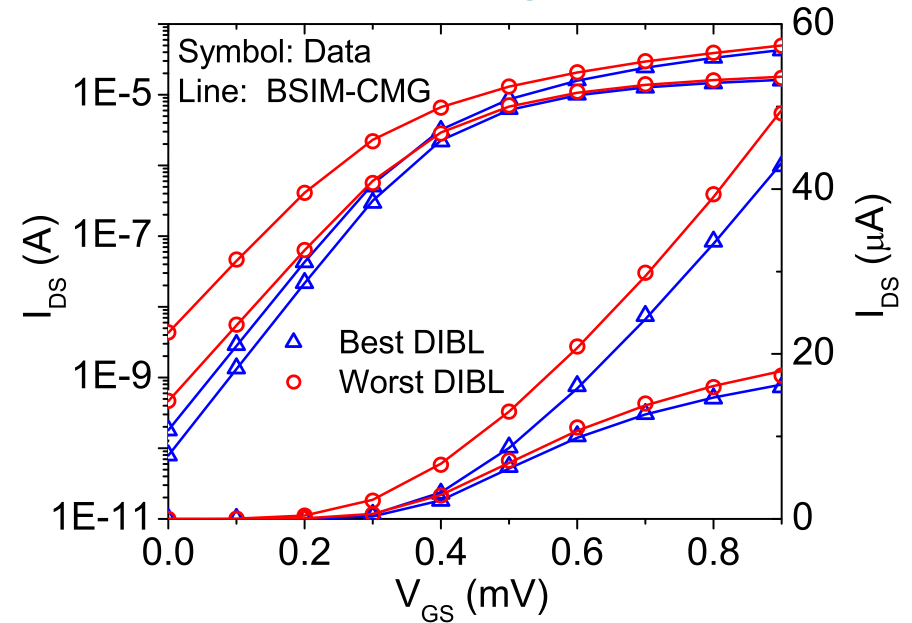






Statistical Compact Modeling

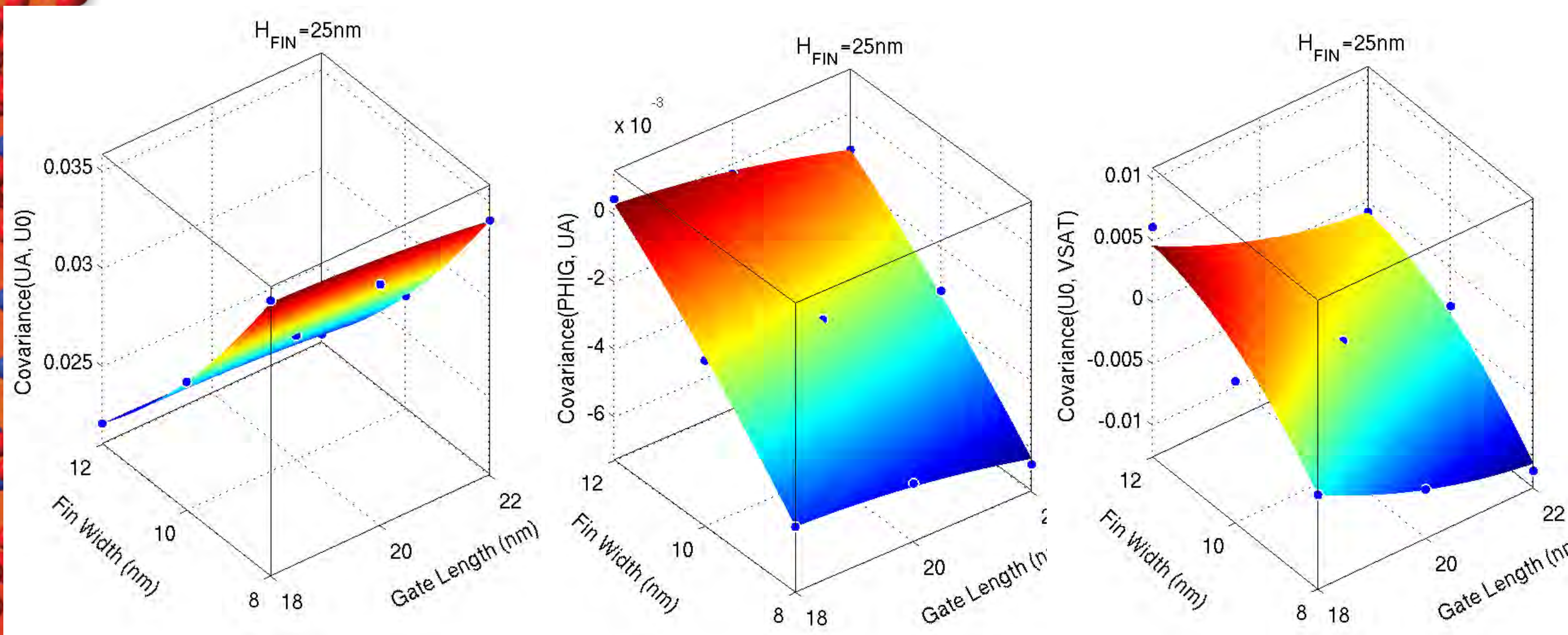




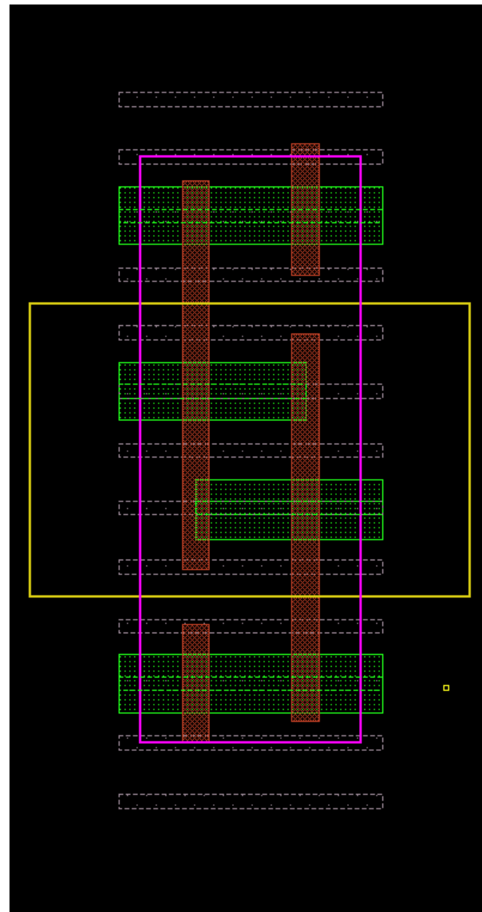
Strong correlation between statistical compact model parameter and device figure of merit demonstrates that extraction is physics based

V_T	-0.895 -0.827	-0.741 -0.743
	I_{ON}	0.617 0.529
		DIBL

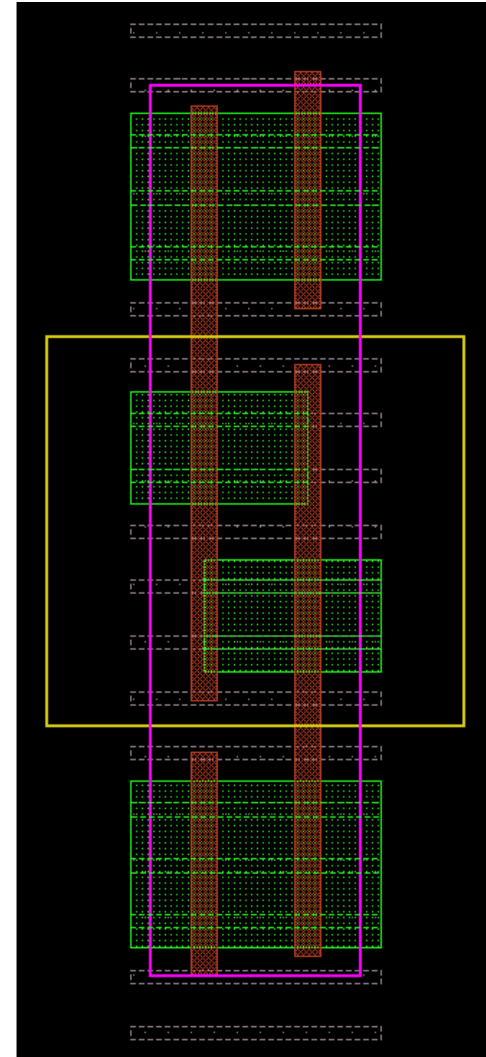
Statistical Compact Modeling – Group 2 parameter



FinFET based SRAM design

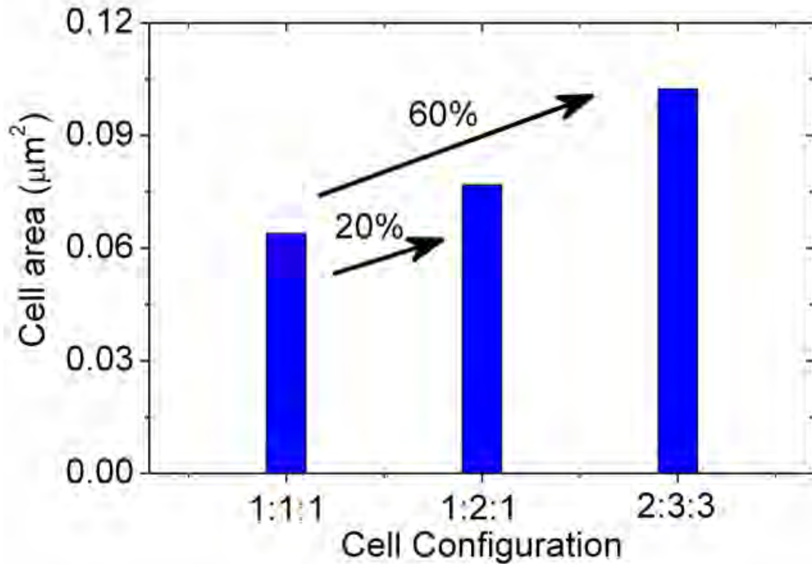


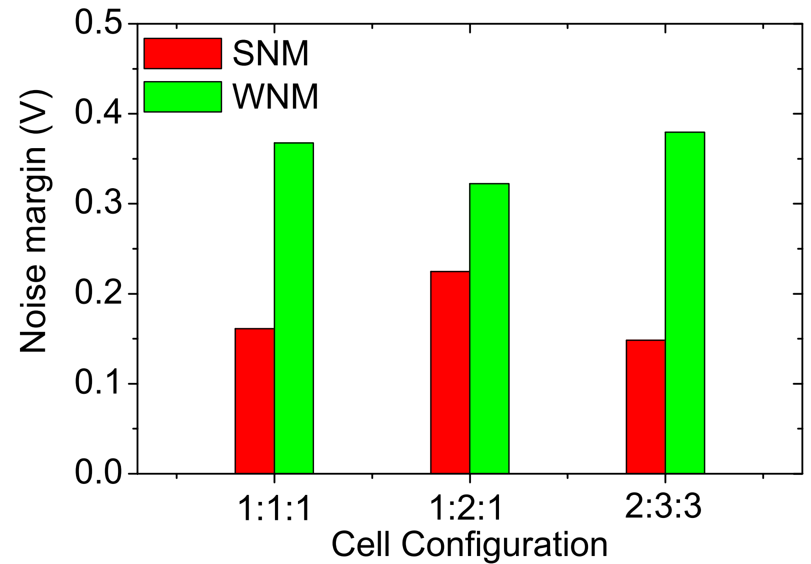
1-1-1 Cell

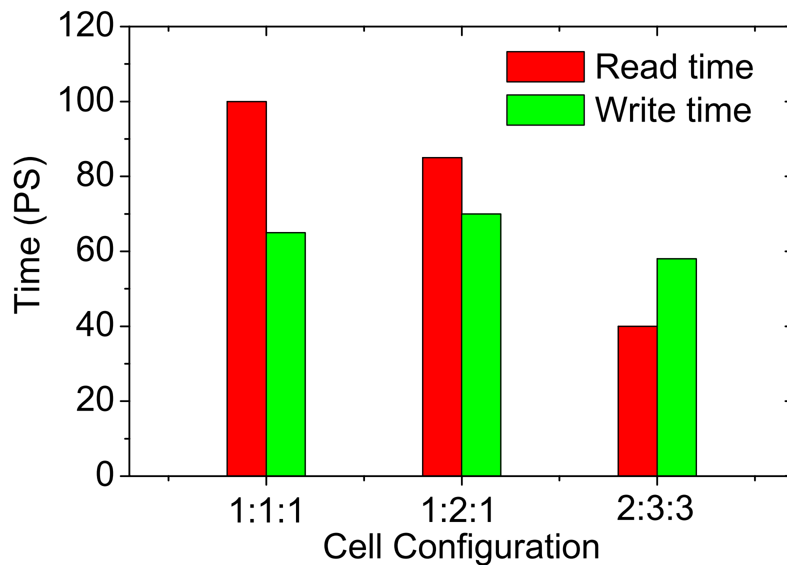


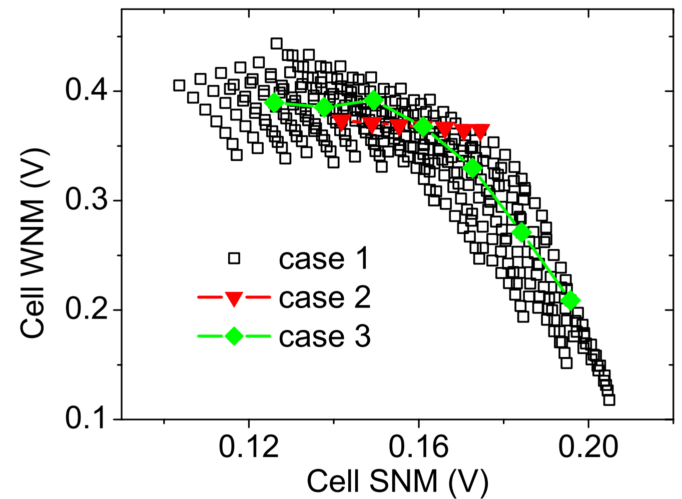
2-3-3 Cell

Cell design trade off



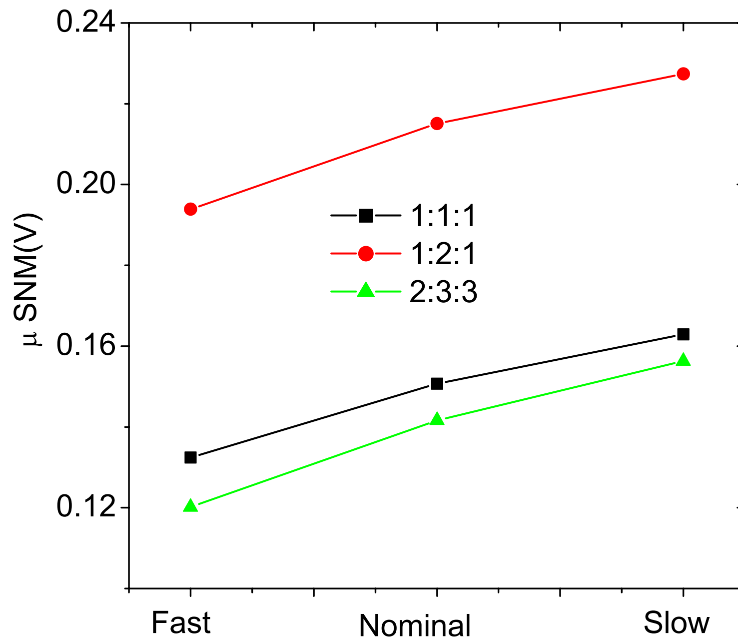


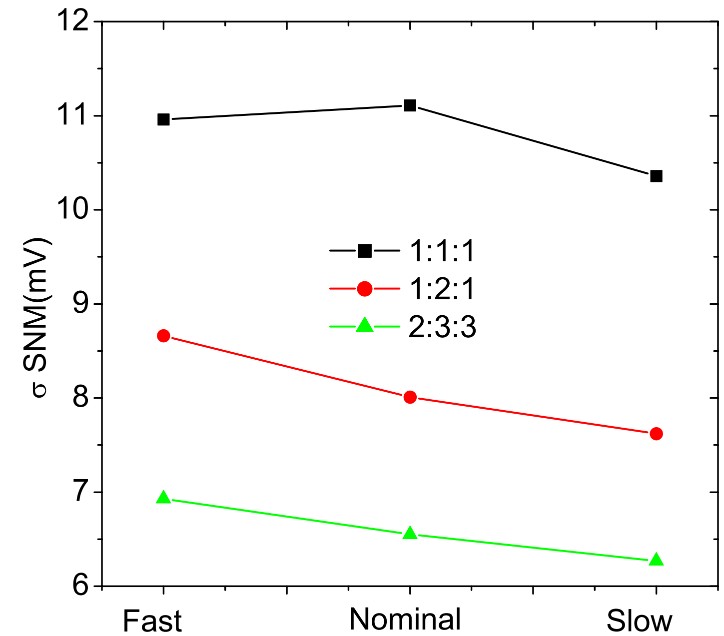


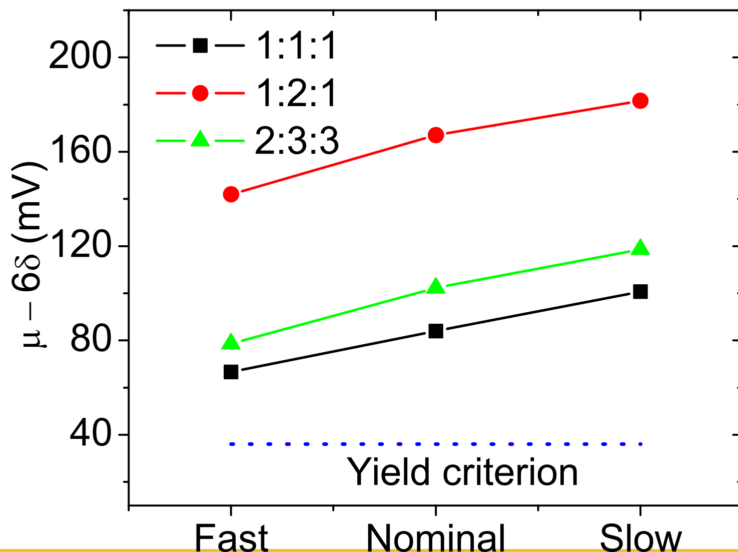


Metal Gate Work-Function Engineering

Interplay between CD and statistical variation

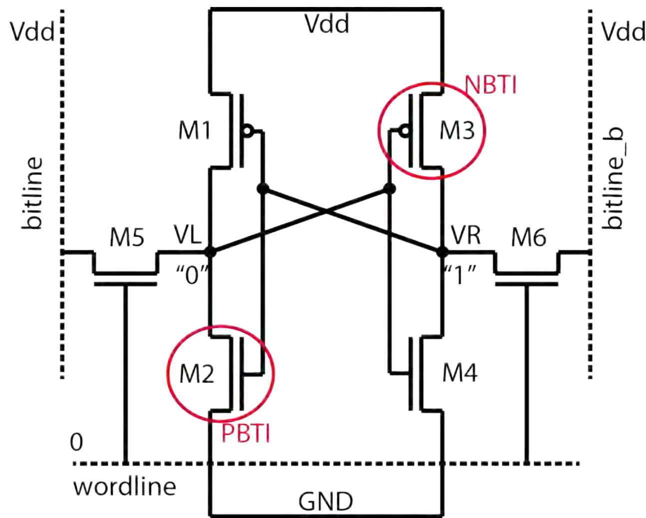


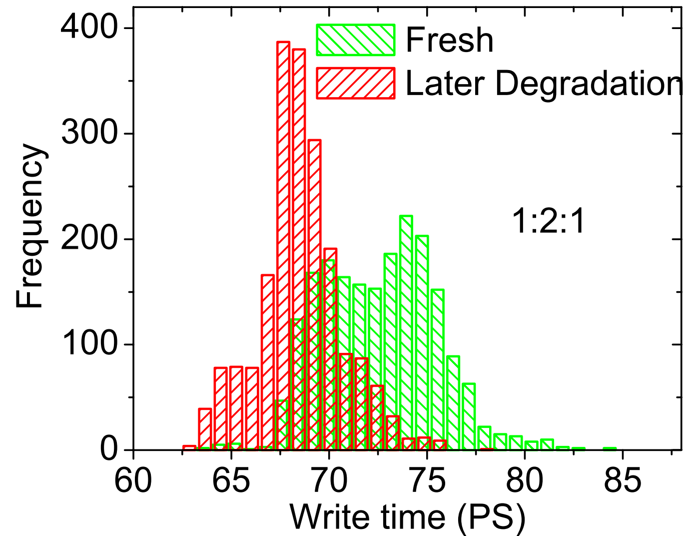


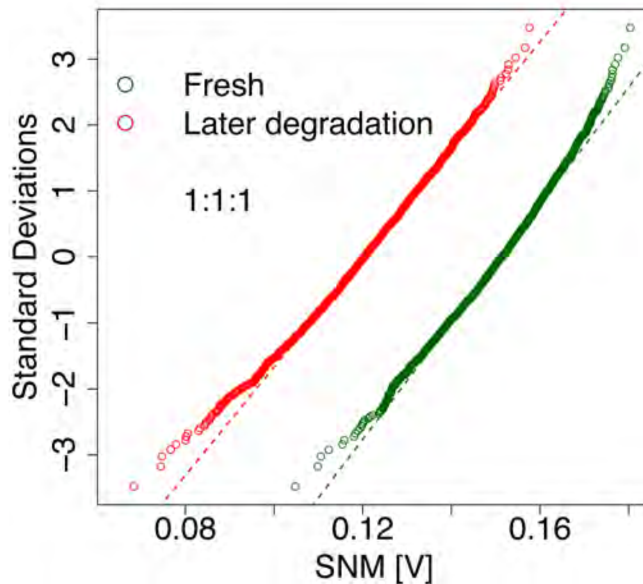


- Slow corner has the best SNM performance.
- CD variation can introduce 10% degradation on standard deviation of SNM.

Reliability Aspect of SRAM Performance





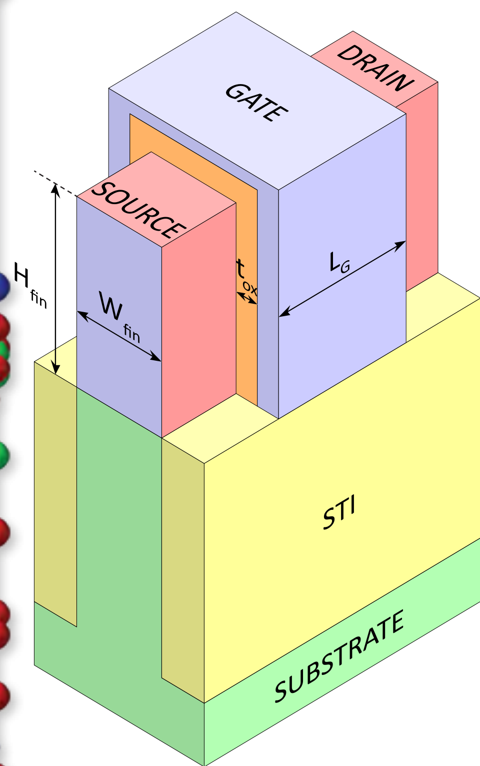


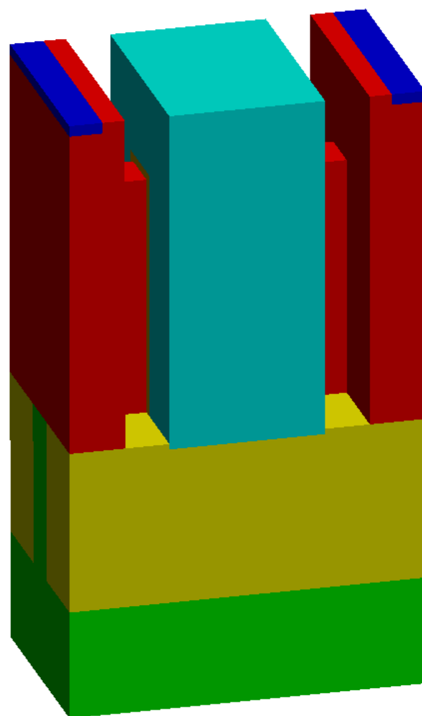
- ➢ Under N/PBTI stress condition, SNM can be degraded by more than 25%
- ➢ However, write operation can be improved under stress condition

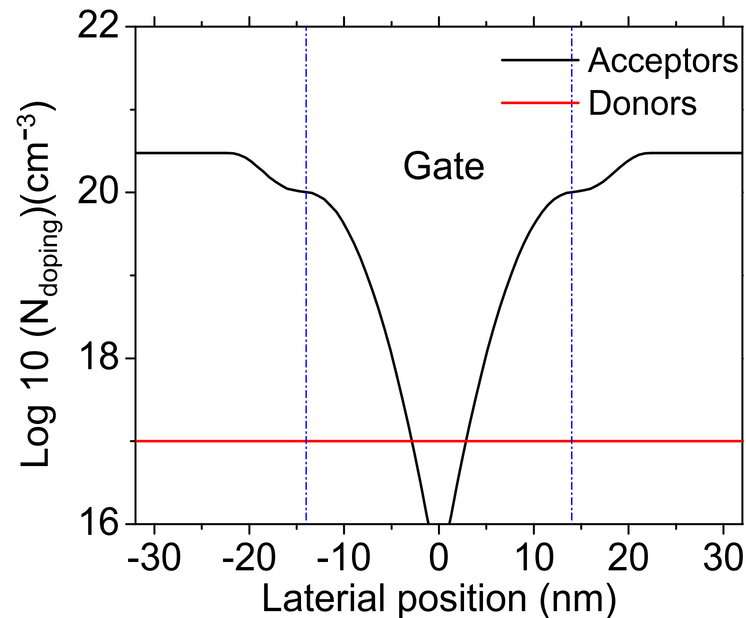
Summary

- Introduction
- 22nm FinFETs: *the Intel benchmark*
- 14nm FinFETs: *Interplay between process and statistical variability*
- 10nm FinFETs: *Si vs. Ge*
- 7nm FinFETs: *the role of III-Vs*
- Conclusions

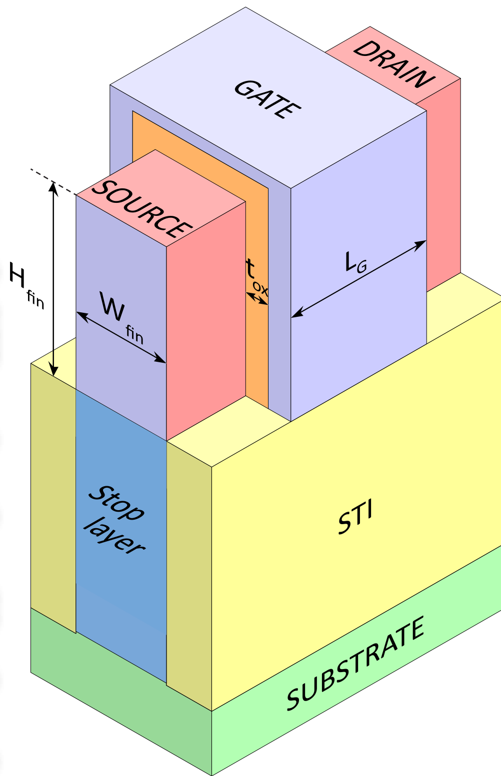
7nm FinFET options: FinFET design

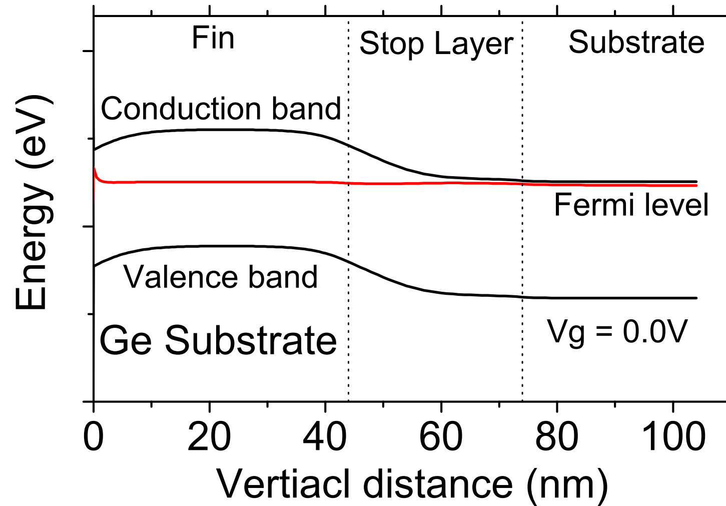


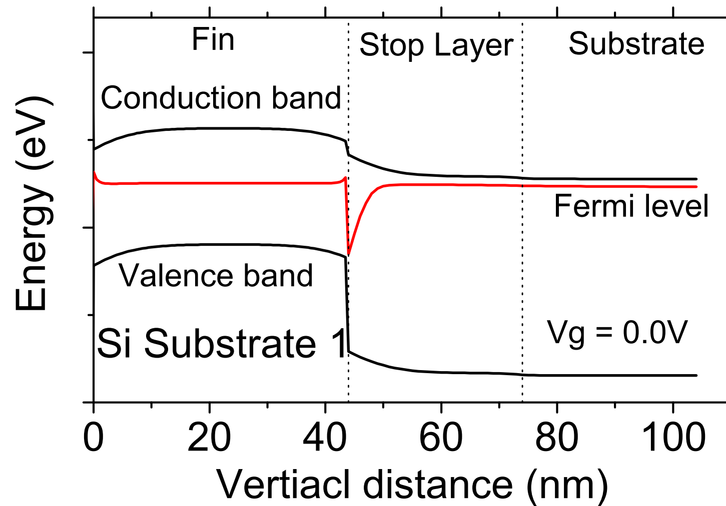




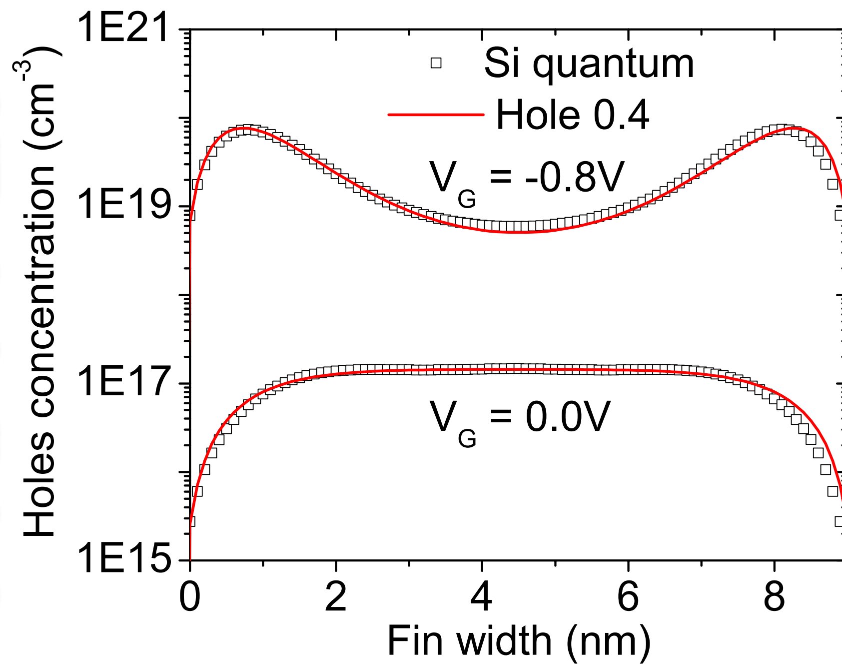
The impact of the stop layer is neglected

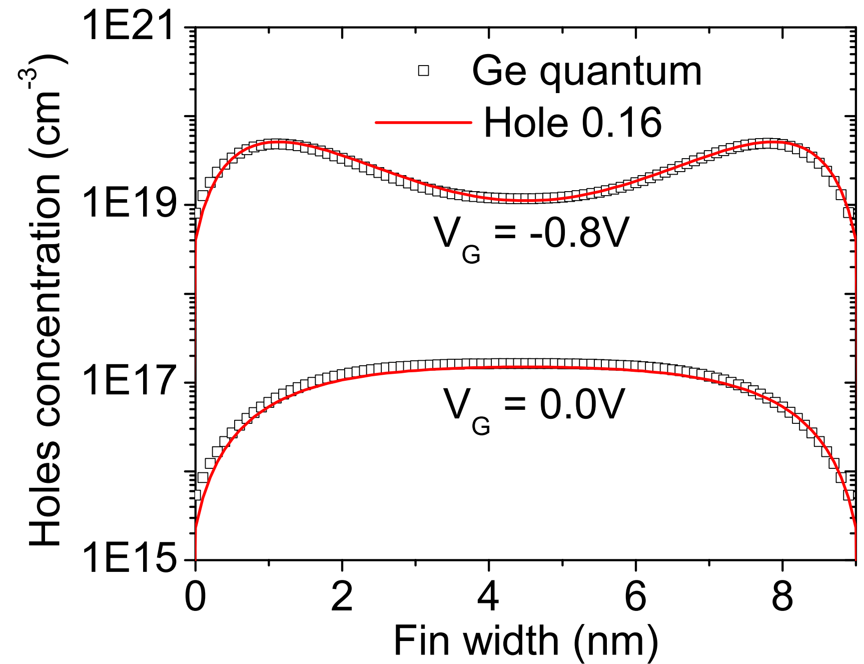




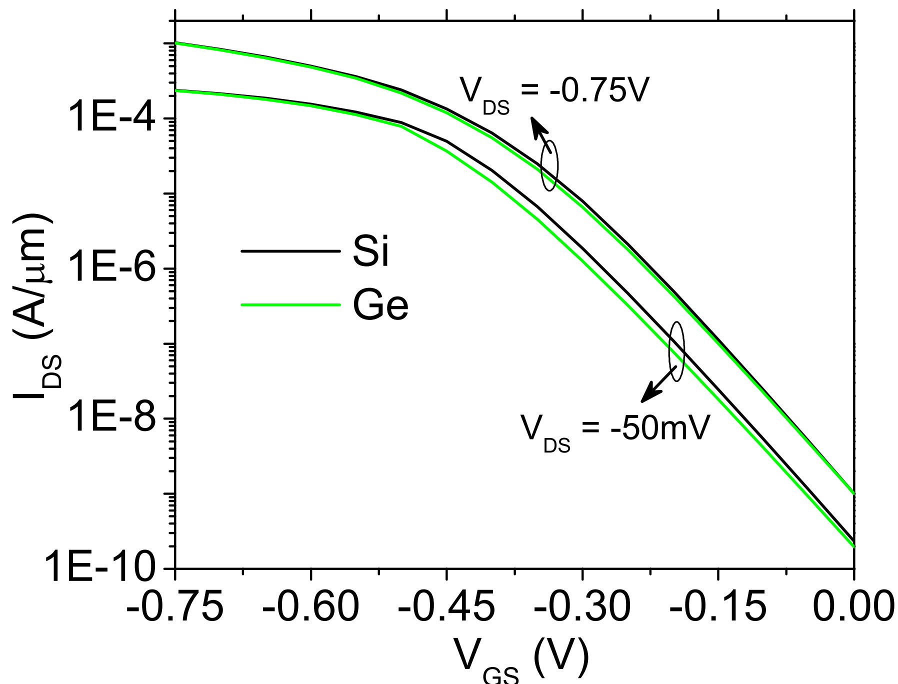


DG quantum corrections
Base on 1D Poisson-Schrodinger solver



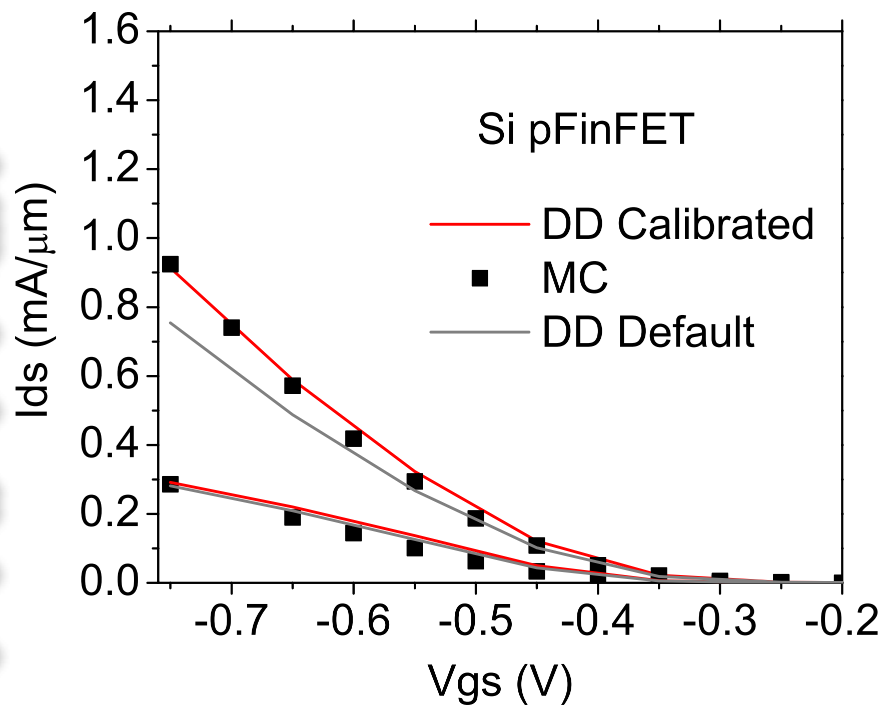


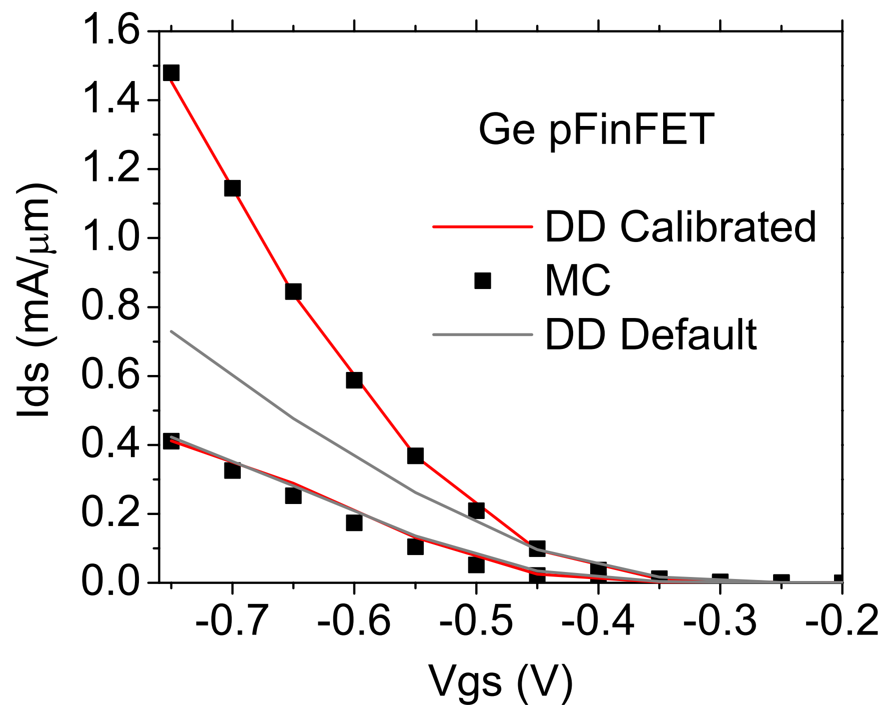
Electrostatic performance based on DD



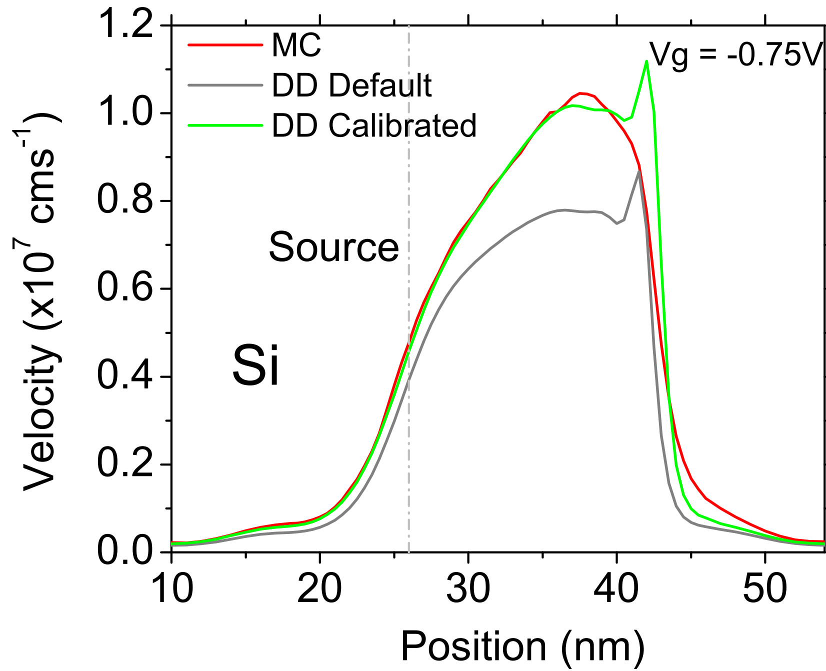
V_{DD} =0.75V	Si pFinFET	Ge pFinFET
Effective mass	0.4	0.16
Work function (eV)	4.664	4.140
DIBL (mV)	51	59
SS (mV)	72	74

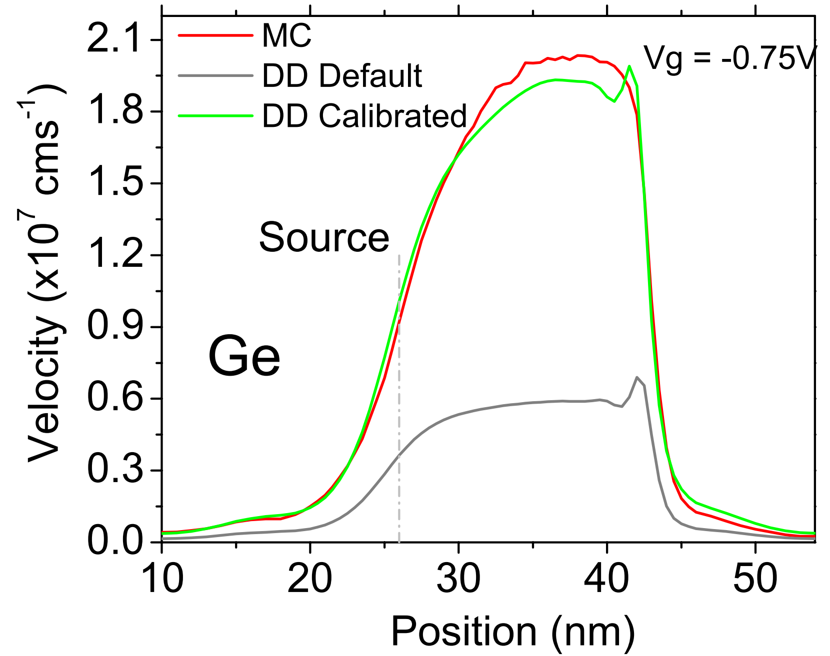
Performance based on MC simulations



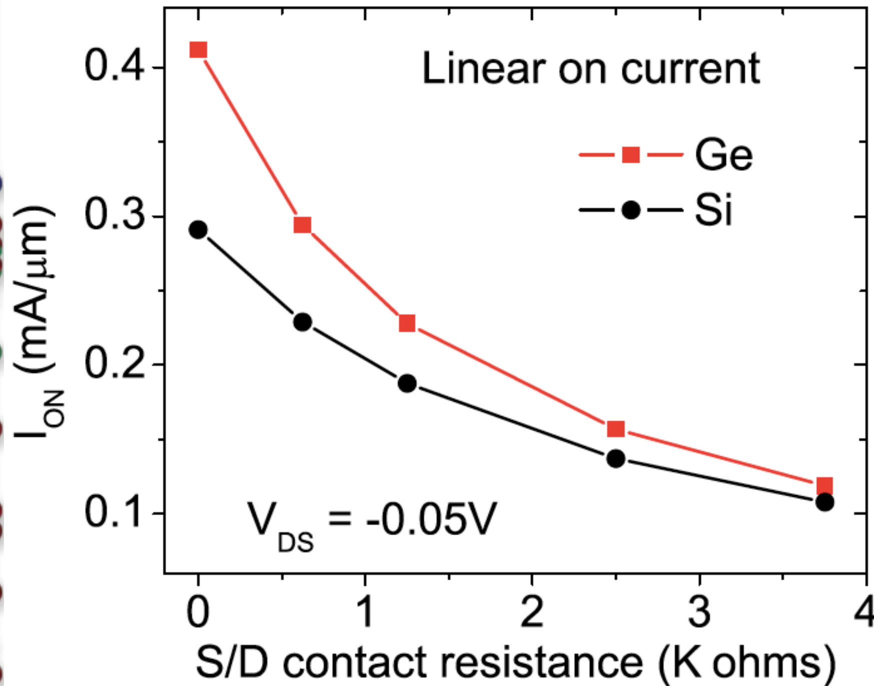


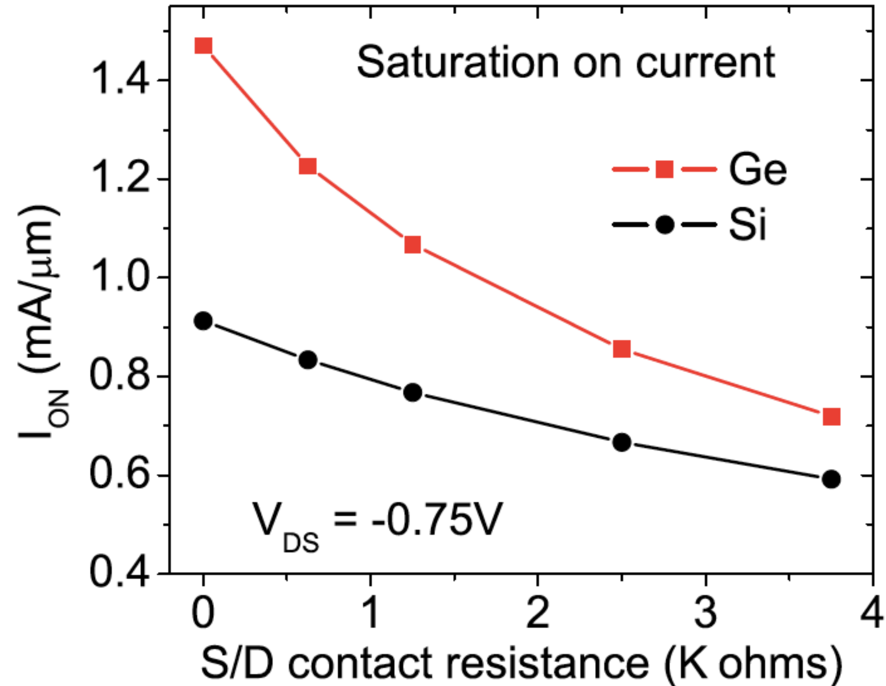
Carrier velocities



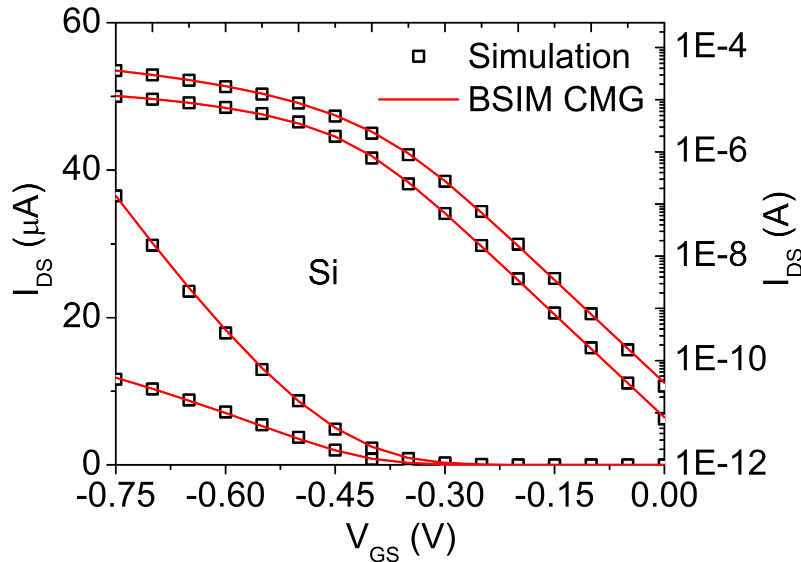


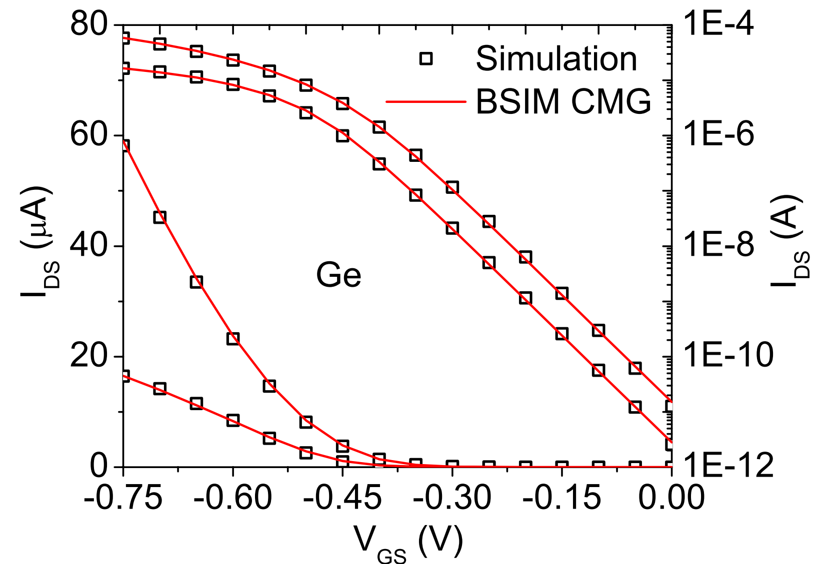
Impact of the contact resistance

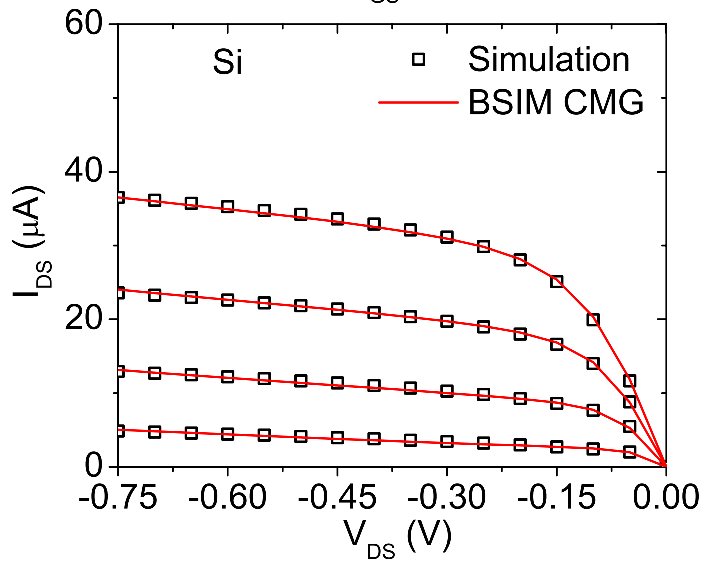


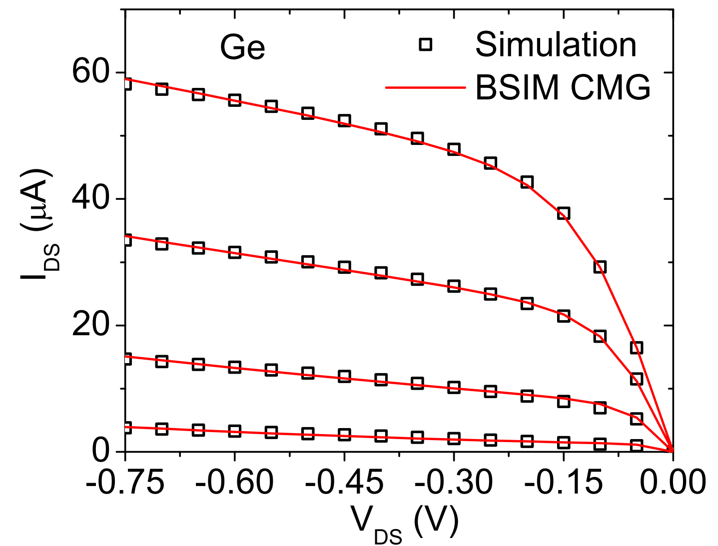


Nominal compact models

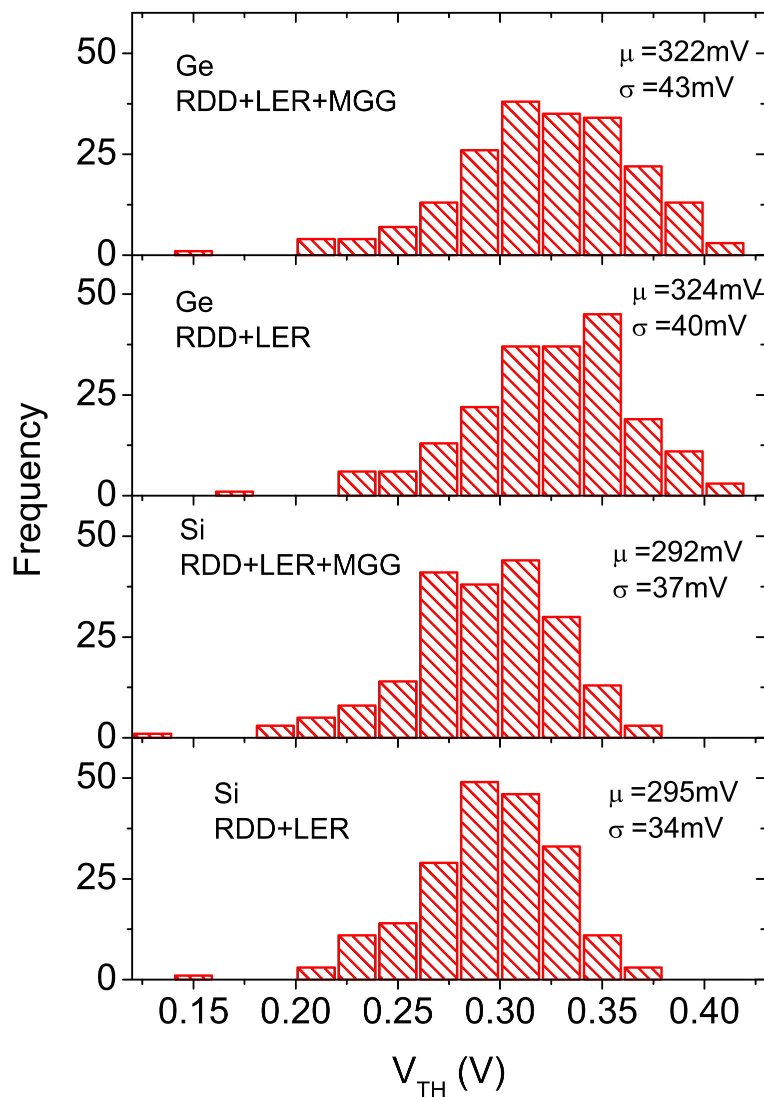


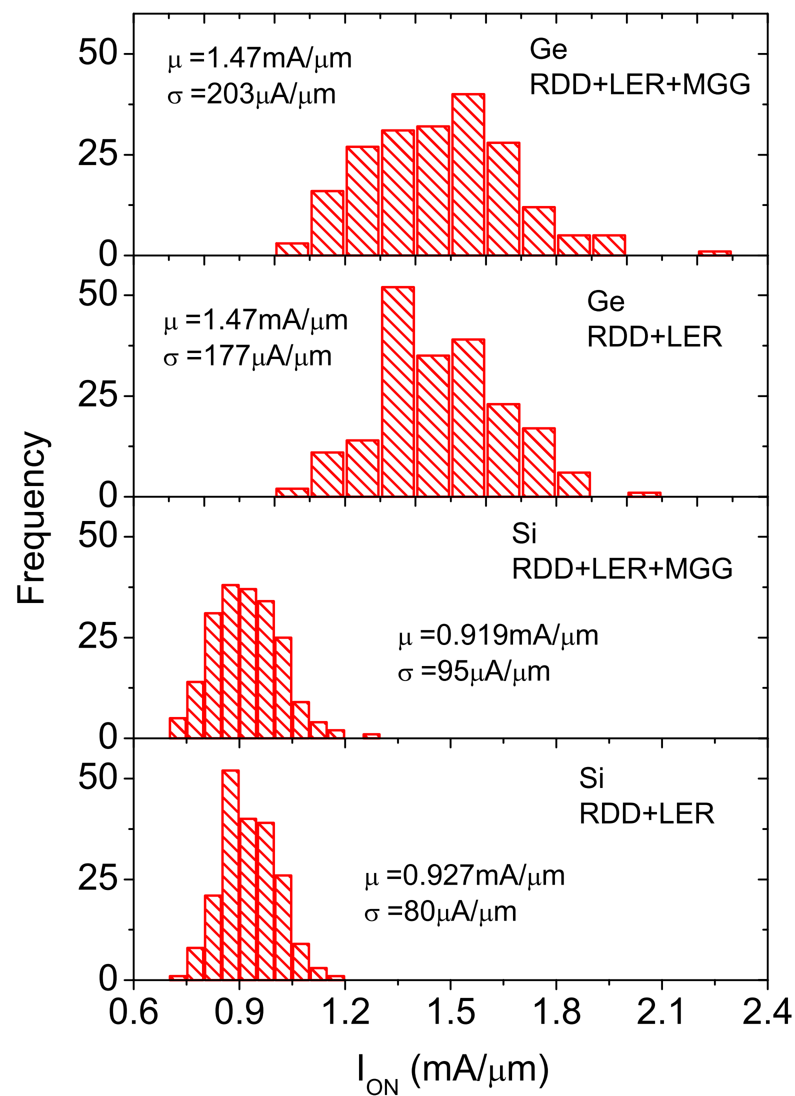




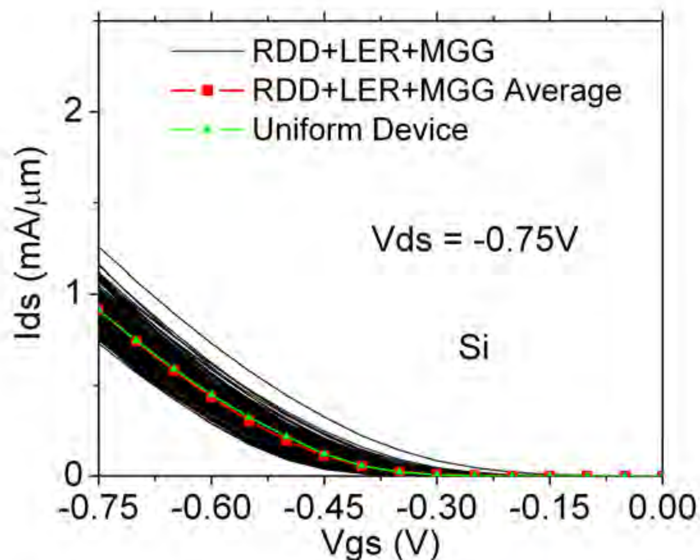


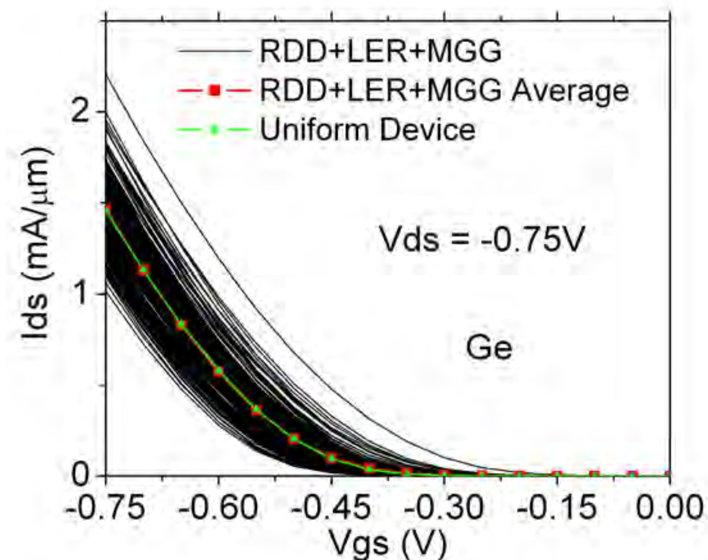
Simulation of statistical variability

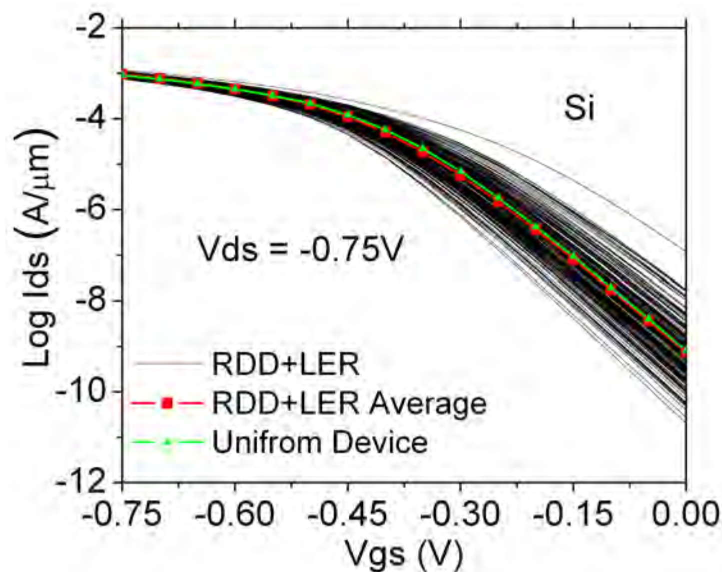


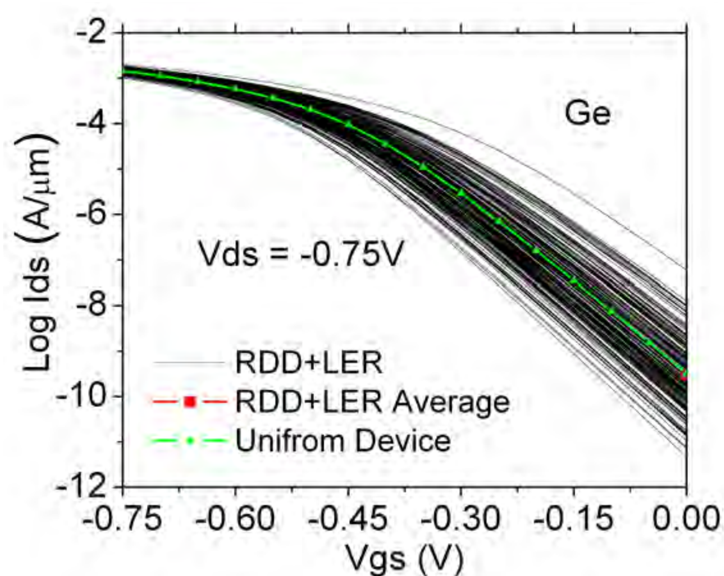


Simulation of statistical variability

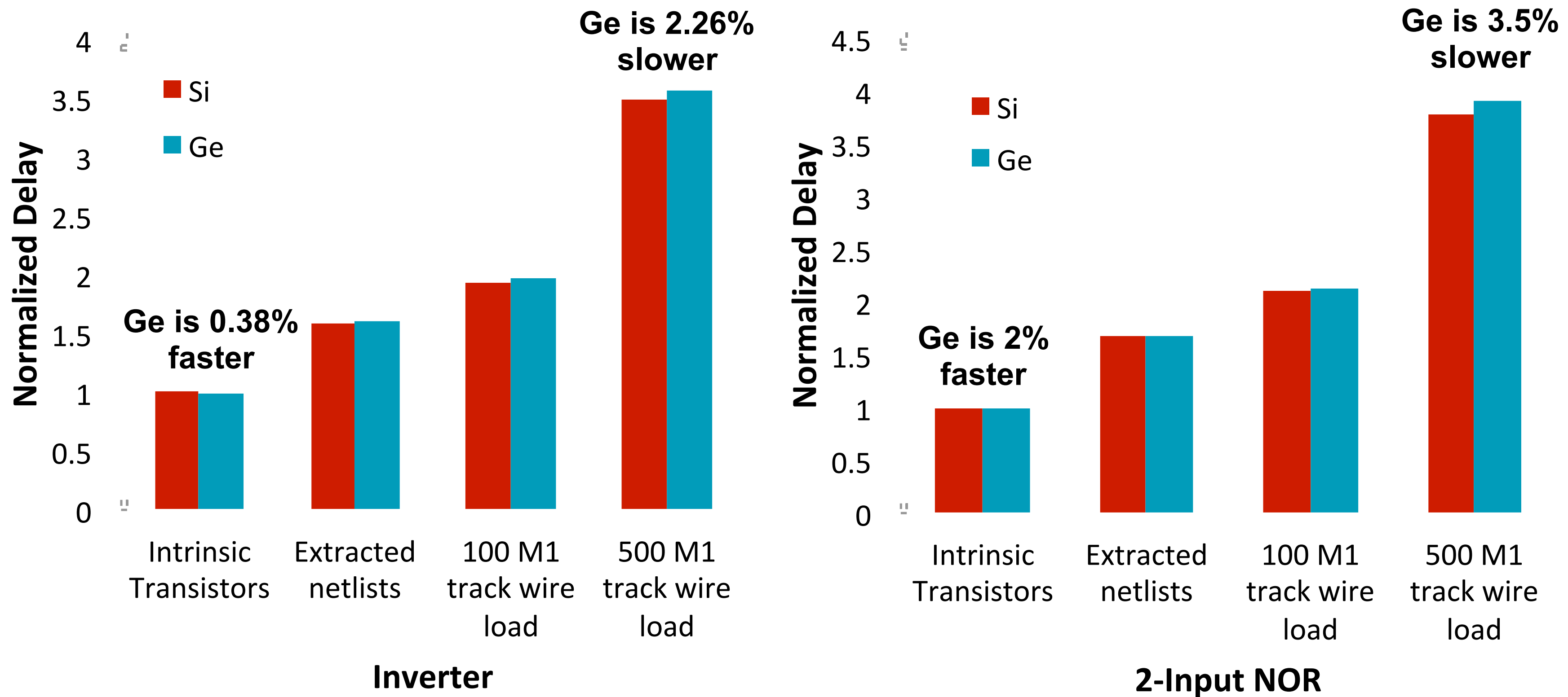






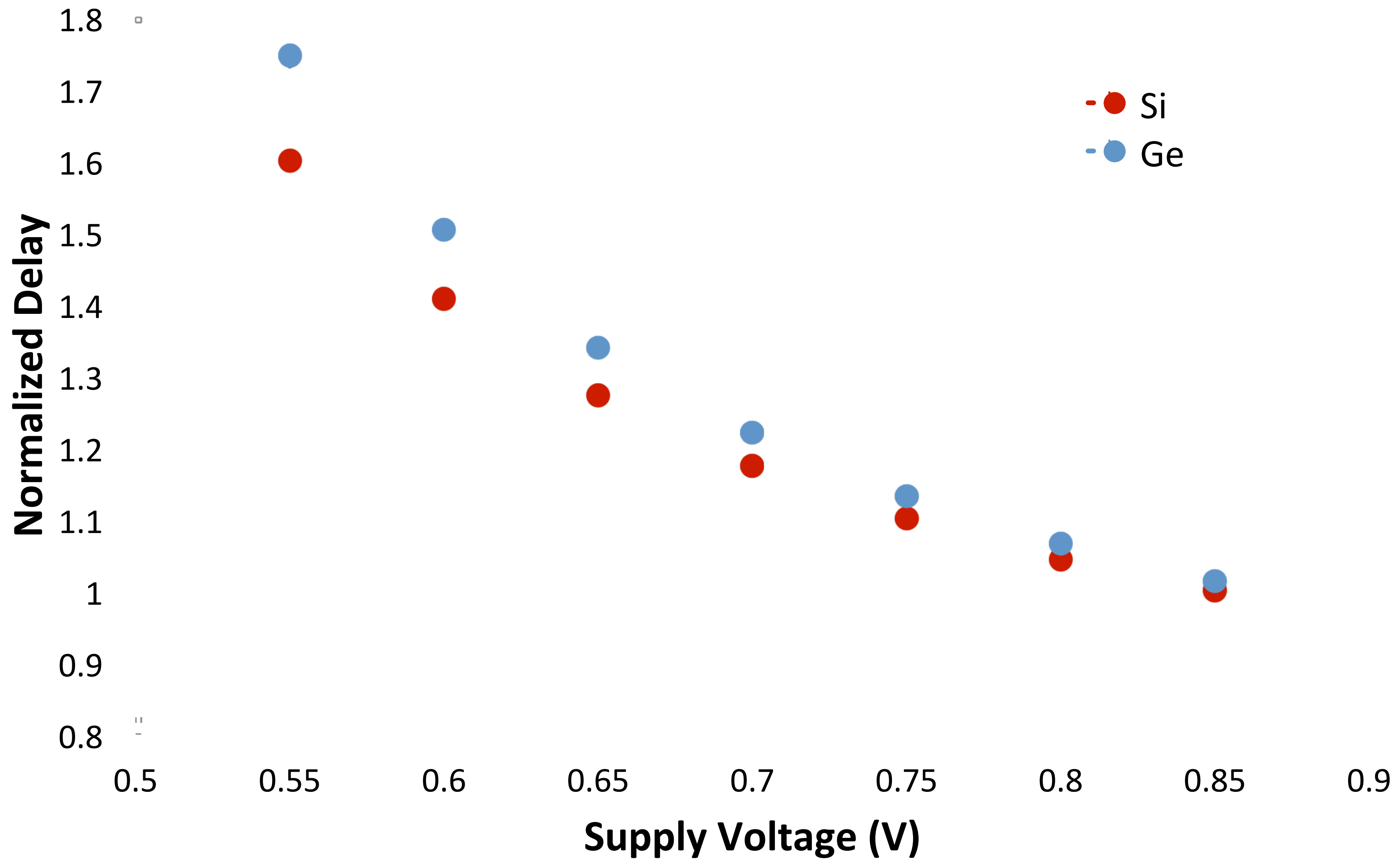


Impact of Extraction and Wire-load



Extracted netlists generated using the ARM 10nm Predictive Technology Modeling toolset

Delay vs. Supply Voltage



Performance vs. Leakage

5

Ge@Ioff=10nA/um
Si@Ioff=10nA/um
Si@Ioff=1nA/um

0.5

Normalized Leakage Power

0.05

0.6 0.7 0.8 0.9 1 1.1 1.2

Normalized Performance

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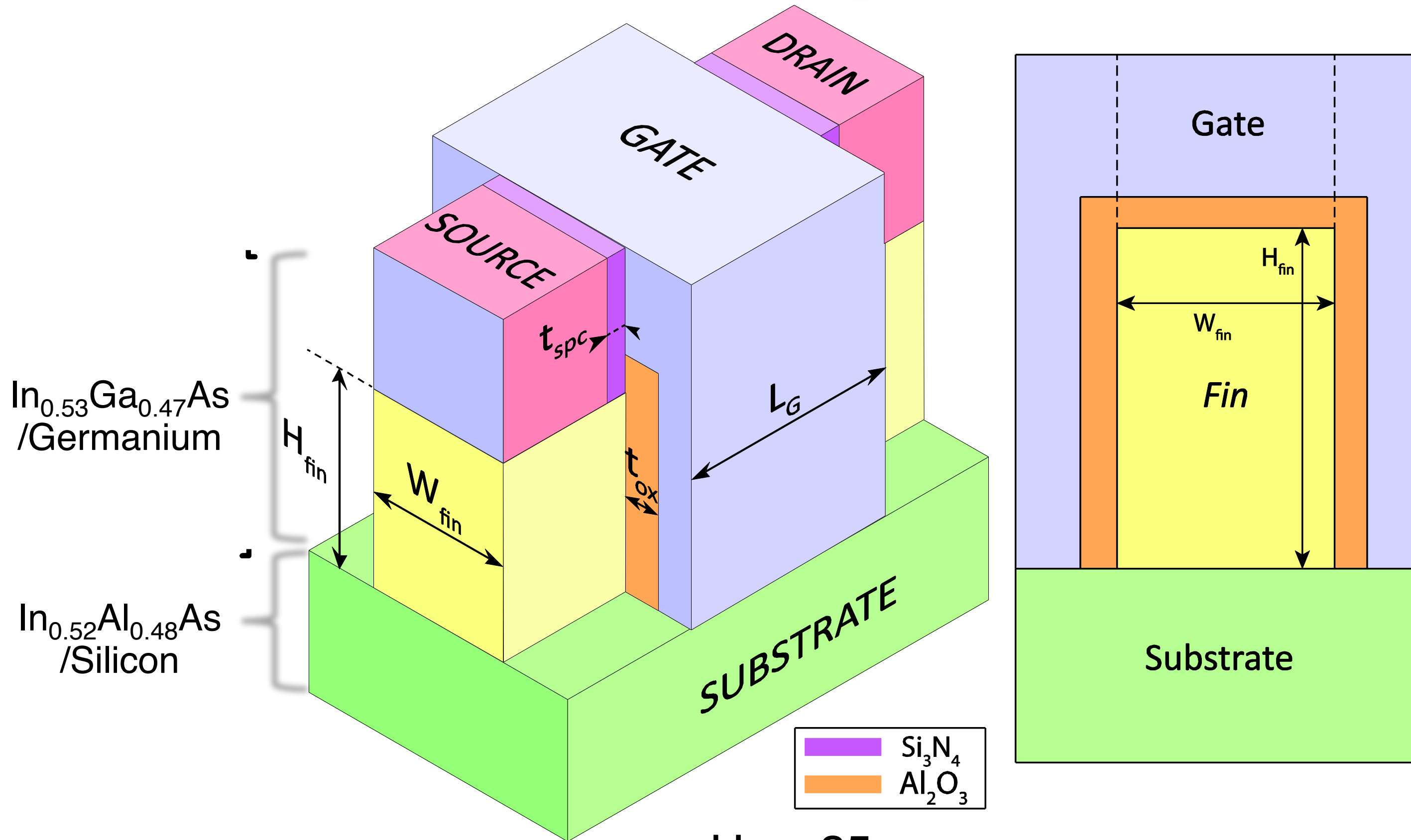
Tri-gate



n-type
SS= 68mV/dec
DIBL= 29mV/V

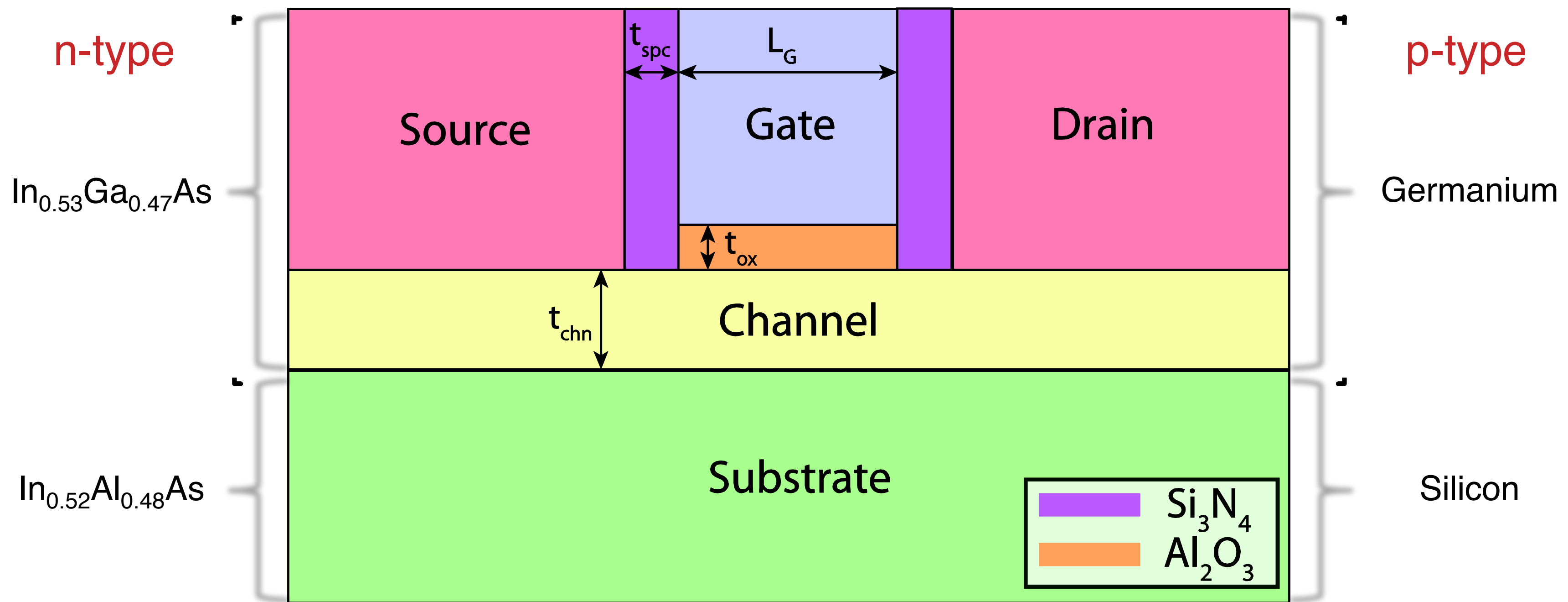
H_{fin}= 25nm
W_{fin}= 10nm
$W_{eff}= 2H_{fin}+W_{fin}$= 60nm

p-type
SS= 69mV/dec
DIBL= 23mV/V

L_G [nm]	EOT [nm]	T_{ox} [nm]	t_{spc} [nm]
15	0.51	1.125	2

Src/Drn [cm^{-3}]	Chn. [cm^{-3}]	Subs. [cm^{-3}]
9.1×10^{19}	1.82×10^{17}	3.65×10^{18}

Implant-Free Quantum-Well



SS= 88mV/dec
DIBL= 85mV/V

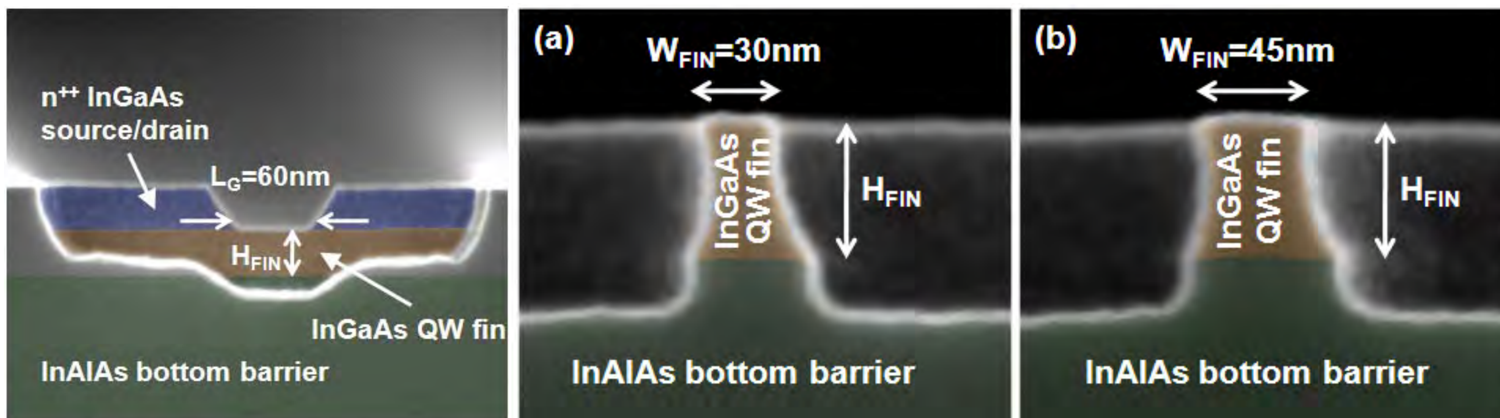
t_{chn}= 3.75nm
W=15nm

SS= 95mV/dec
DIBL= 70mV/V

L_G [nm]	EOT [nm]	T_{ox} [nm]	t_{spc} [nm]
15	0.51	1.125	2

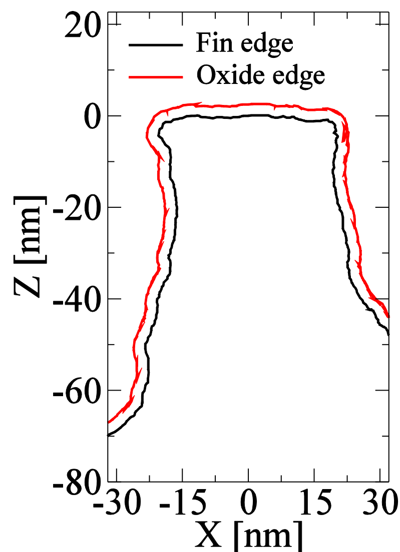
Src/Drn [cm^{-3}]	Chn. [cm^{-3}]	Subs. [cm^{-3}]
9.1×10^{19}	1.82×10^{17}	3.65×10^{18}

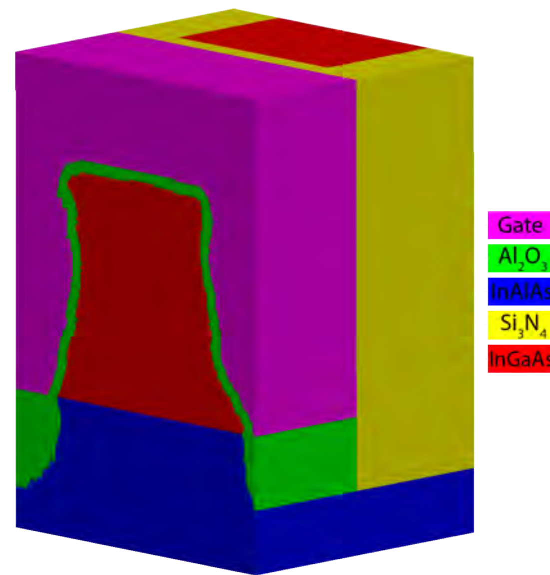
Fin Profile Extraction



M. Radosavljevic et al., Tech. Dig.-Int. Electron Devices Meet., 2011, 33.1

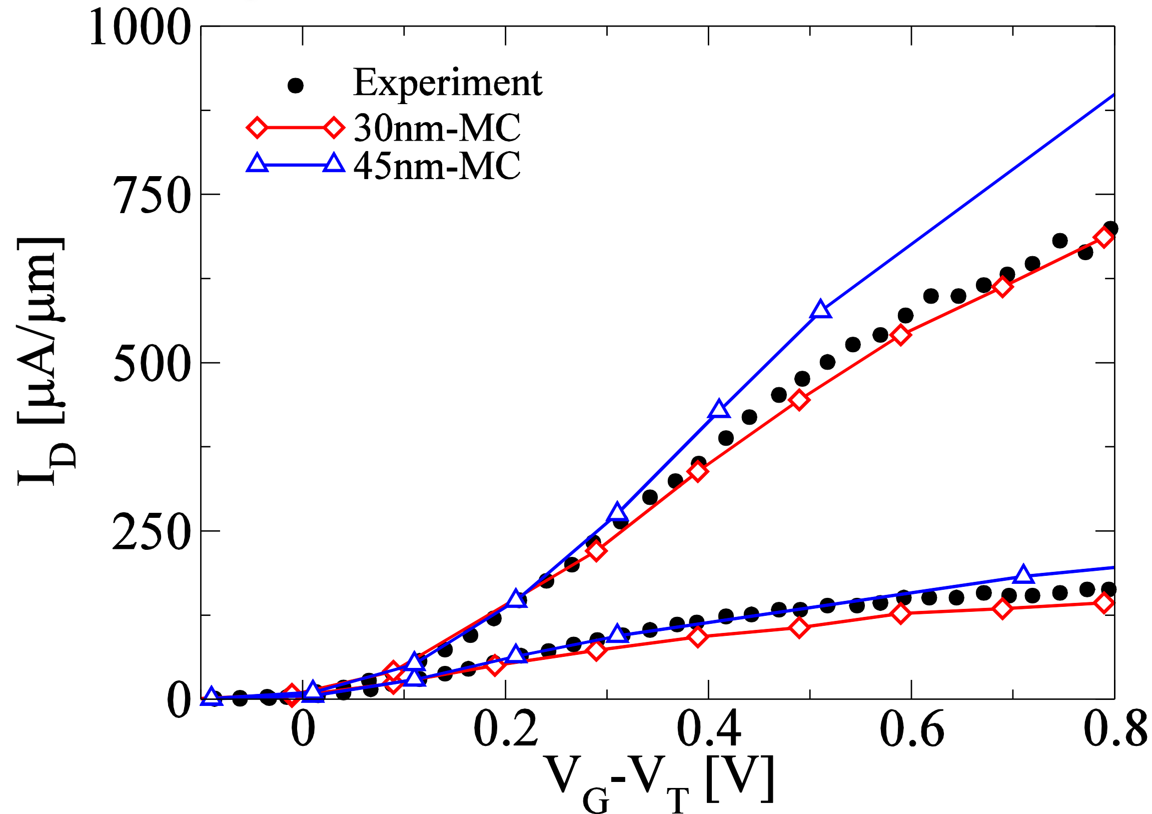
- Extract fin profiles for both W_{fin} from published data.
- Import the fin profiles into the simulation domain.
- Use published structure parameters: L_G=60nm, t_{spc}=5nm, EOT=12Å, H_{fin}=50nm.





W_{fin}=45nm

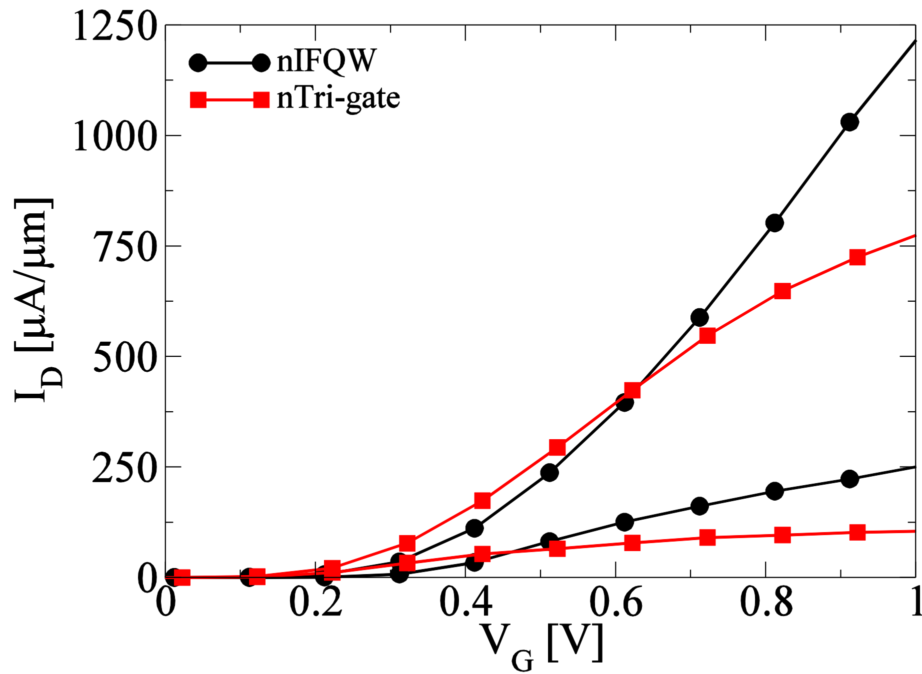
Experimental Verification

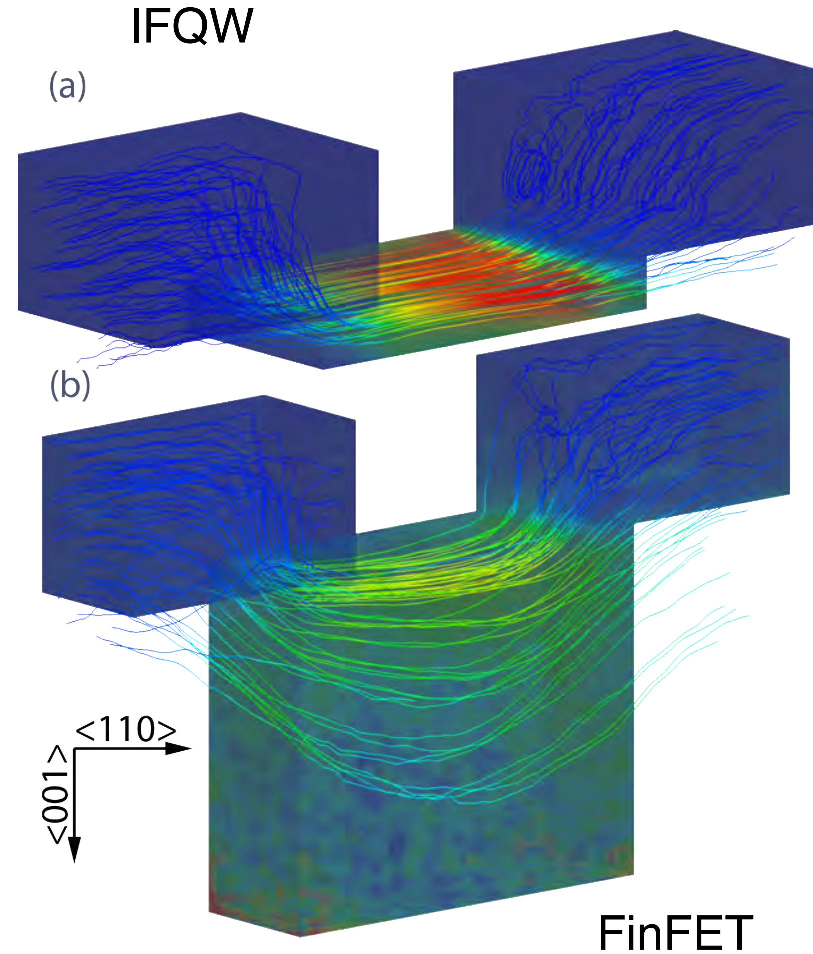


- Gate work-function calibrated using drift-diffusion.
- Published I_D-V_G data has W_{fin}=40nm.
- Extracted fin profiles bracket published results.
- Simulations without interface roughness scattering.
- Monte Carlo shows excellent agreement.

M. Radosavljevic et al., Tech. Dig.-Int. Electron Devices Meet., 2011, 33.1

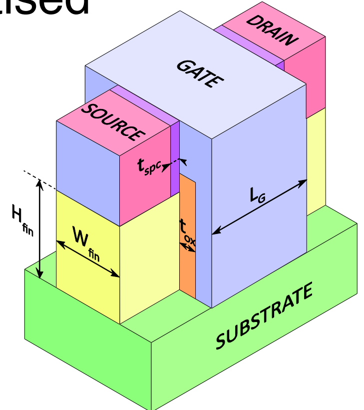
7nm CMOS device performance



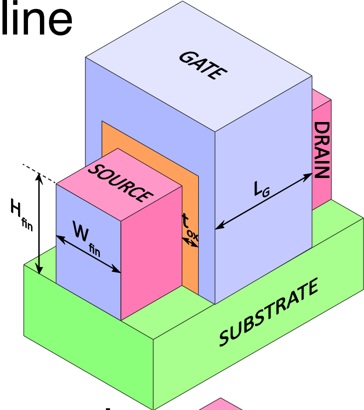


III-V FinFET performance

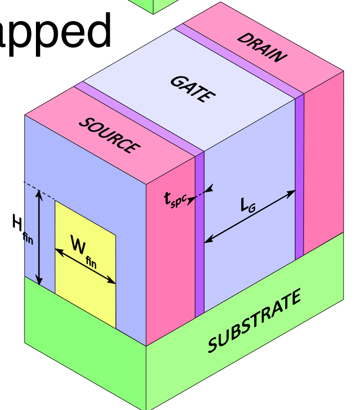
Raised



Inline



Wrapped



I_D [μA/μm]

1000
800
600
400
200
0

0 0.1 0.2 0.3 0.4 0.5

(V_G-V_T) [V]

Raised S/D
Inline S/D
Wrapped S/D

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- There is a strong interplay between process and statistical variability in advanced technologies.
- Compact models should capture acurately this interplay.
- Hi level of automation and accuracy is needed from the simulation tool to enable DTCO.
- DTCO is crucial for both Foundries, IDMs and fables companies

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